

Design of Area-Efficient, Low-Quiescent-Current LDOs for Chip-Level Power Management

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Abstract - In this paper, design methodology of area-efficient and low-quiescent-current low-dropout regulators (LDOs) for chip-level power management is proposed. As LDO chip size is dominated by the large size power transistor, guidelines are given to minimize its size when design specifications such as the dropout voltage, the minimum input voltage and the maximum load current are given. The reduced power transistor size also helps to maintain satisfactory error amplifier slew-rate at low quiescent current consumption. Stability of LDO designed under the proposed methodology is thoroughly studied. Extensive simulations are done to verify the stability study.

I. INTRODUCTION

Recently, chip-level power management with embedded low-dropout regulators (LDOs) has drawn a great attention among the electronic industry and research community [1-2]. To minimize the chip size and power consumption, the embedded LDOs should have high area efficiency and low quiescent current consumption. However, most of LDOs [3-7] are developed with the use of a large value output capacitor that is normally ranged from few hundreds nF to several tens of μF . Integrating such large value output capacitor with LDOs for chip-level power management is definitely not an area-efficient approach. To develop LDOs with very small output capacitance that is mainly contributed by the metal routing used for chip-level power distribution, different LDO topologies have been proposed [4 & 8]. Even those topologies can greatly minimize the total value of on-chip compensation capacitors, the use of on-chip capacitors still inevitably degrades LDO area efficiency that is very important in applications [1-2] where multiple LDOs are used. Recently, an area-efficient LDO has been proposed for microprocessor application [9]. As fast load regulation is required, the quiescent current of LDO in [9] is around 6-mA at 100-mA full load current (e.g. $\sim 94\%$ current efficiency). However, this current efficiency is a little bit too large for LDOs used in battery-powered mobile systems.

In this paper, design of area-efficient and low-quiescent-current LDOs is thoroughly discussed. Section II presents the design methodology of LDOs with high area efficiency and low quiescent current consumption. Stability of such LDOs is carefully studied in Section III. Finally, conclusion is given in Section IV.

II. DESIGN OF AREA-EFFICIENT AND LOW-QUIESCENT-CURRENT LDOs

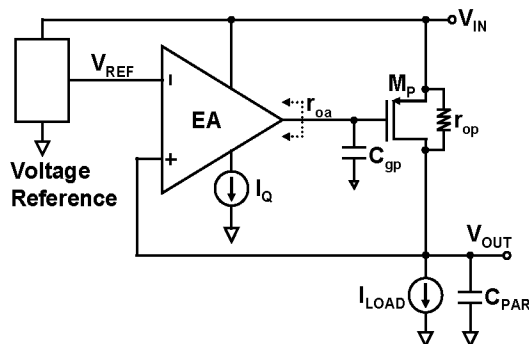


Fig. 1 Schematic of a generic LDO.

Fig. 1 shows a generic LDO consisting of an error amplifier (EA), a PMOS power transistor (M_P), and a voltage reference that can be bandgap reference [10-13]. Small signal elements are included in Fig. 1 for the stability analysis in Section III. The current source (I_{LOAD}) is used to model the current consumed by the load circuit. Another current source (I_Q) is used to illustrate that quiescent current is defined as the current consumed by the control circuit of LDO (e.g. EA) but not the current delivered by the power transistor to load (e.g. I_{LOAD}).

To reduce the quiescent current without degrading the error amplifier slew-rate (SR), which is defined as the I_Q divided by the gate capacitance of power transistor (C_{gp} , e.g. $SR=I_Q/C_{gp}$), the size of power transistor should be minimized such that the C_{gp} can be reduced. Moreover, chip size of LDO is dominated by the large size power transistor. Minimizing the size of power transistor not only improves LDO area efficiency, it also improves SR of error-amplifier without increasing the I_Q of LDO.

The size of power transistor can be minimized by designing it to operate in linear region at a given dropout voltage (V_{DO}), which is defined as the minimum pass-transistor source-to-drain voltage to maintain output voltage regulation at maximum load current (I_{LOAD_MAX}) and minimum input voltage (V_{IN_MIN}). Size or aspect ratio (W_p/L_p) of power

transistor can be calculated with equation (1) shown in the following

$$\frac{W_p}{L_p} = \frac{I_{LOAD_MAX}}{\mu_p C_{OXp} V_{DO} (V_{IN_MIN} - V_{OEA_MIN} - |V_{THP}| - V_{DO}/2)} \quad (1),$$

where μ_p , C_{OXp} , and V_{THP} , are mobility, gate capacitance per unit area, and threshold voltage, of M_p , respectively. As illustrated in Fig. 2, the term V_{OEA_MIN} is the minimum error amplifier output voltage at which the error amplifier is still operated in high-gain region. To minimize the V_{OEA_MIN} such that the aspect ratio of power transistor can be further minimized, transistors at the output of error amplifier should be designed to have small drain-to-source saturation voltage. This can be achieved by designing the output transistors with very small overdrive voltage. Although small overdrive voltage requires the output transistors with large aspect ratio, which unavoidably increases the internal node capacitance of error amplifier, slew-rate of error amplifier is not degraded as its slew-rate is limited at its output by the gate capacitance of M_p . Power transistor worked in linear region may degrade the loop gain and hence the regulation performance of LDO operated at the dropout situation. However, it saves huge chip area compared to LDOs with power transistor operated in saturation region. Table I summarizes the aspect ratio of power transistor designed by the “linear region” approach and the “saturation region” approach at different CMOS technologies where transistor parameters are obtained at [14]. The V_{DO} , V_{IN_MIN} , V_{OEA_MIN} , and I_{LOAD_MAX} are assumed to be 0.2V, 1.2V, 0.1V, and 50mA, respectively.

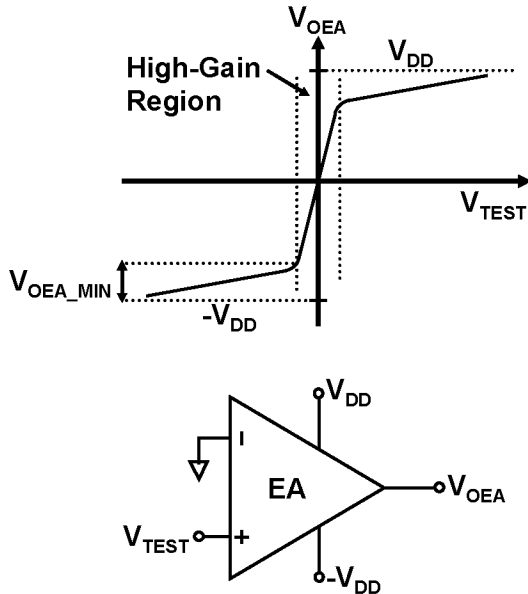


Fig. 2 Graphical illustration of V_{OEA_MIN} that is defined as the minimum error amplifier output voltage at which the error amplifier is still operated in high gain region.

TABLE I

ASPECT RATIO OF M_p WITH “LINEAR REGION” APPROACH AND “SATURATION REGION” APPROACH AT DIFFERENT CMOS TECHNOLOGIES.

CMOS Technology	Aspect Ratio at “Linear Region” Approach	Aspect Ratio at “Saturation Region” Approach
0.13- μ m	~5500	~25640
0.18- μ m	~6800	~29300
0.25- μ m	~10400	~41600

III. STABILITY ANALYSIS

To analyze stability of LDO shown in Fig. 1, loop-gain analysis is performed in this section. It is found that there are two left-half-plane (LHP) poles

$$P_{OEA} = \frac{1}{r_{oa} \cdot C_{gp}} \quad (2)$$

and

$$P_{OLDO} = \frac{1}{r_{op} \cdot C_{PAR}} \quad (3),$$

where r_{oa} is the output resistance of error amplifier and r_{op} is the drain resistance of power transistor. C_{PAR} is the parasitic capacitance at the output of LDO contributed by the metal routing used for chip-level power distribution. The pole P_{OEA} is formed at the output of error amplifier and the pole P_{OLDO} is at the output of LDO. The pole P_{OEA} is located at much lower frequency than the pole P_{OLDO} . This is because the r_{oa} is much larger the r_{op} due to the fact that channel length of transistors used in error amplifier is normally several times larger than the minimum feature size of a given CMOS technology but channel length of power transistor follows the minimum feature size for smaller chip size. Moreover, the C_{gp} and the C_{PAR} is normally in the same order of magnitude (e.g. ~pF). The corresponding locations of poles P_{OEA} and P_{OLDO} are illustrated in Fig. 3. The location of pole P_{OEA} is relatively fixed. However, the pole P_{OLDO} has a strong dependence on load current (e.g. $r_{op} \propto 1/I_{LOAD}$). When load current is large, stability of LDO is guaranteed as the pole P_{OLDO} is located far away from the pole P_{OEA} and the unity-gain frequency (f_{UG}). Equation (4) gives the f_{UG} expression

$$f_{UG} = \frac{g_{ma} g_{mp} r_{op}}{C_{gp}} \quad (4),$$

where the g_{ma} and the g_{mp} are transconductance of error amplifier and power transistor, respectively. When load

current is reduced, the pole P_{OLDO} is moved from high frequency regime to low frequency region. Once the P_{OLDO} becomes smaller than the f_{UG} , LDO stability is very difficult to guarantee. In other words, the LDO is stable when the pole P_{OLDO} is larger than the f_{UG} . Equation (5) shows this stability criterion (e.g. $P_{OLDO} > f_{UG}$) by using the equations (3) and (4)

$$\frac{C_{gp}}{C_{PAR}} > g_{ma}r_{op}g_{mp}r_{op} \quad (5).$$

The term at right-hand-side of (5) has very strong dependence on load current [e.g. $g_{ma}r_{op}g_{mp}r_{op} \propto 1/(I_{LOAD})^{3/2}$]. Stability of LDO can only be guaranteed down to certain value of load current. Large C_{PAR} caused by the on-chip metal routing for power distribution also hurts LDO stability. Although a larger C_{gp} due to the use of larger size power transistor helps to improve LDO stability, chip area efficiency is inevitably increased.

To quantitatively evaluate stability of LDO at different load-current levels, extensive simulations are done at 0.13- μm CMOS technology. The error amplifier shown in Fig. 4 is used in the simulations. The current source I_Q of that amplifier is around $10\mu\text{A}$ such that the quiescent current of LDO is around $20\mu\text{A}$. Channel length of transistors in that error amplifier is designed to be four times the minimum feature size of 0.13- μm CMOS technology (e.g. $L=0.52\mu\text{m}$). The aspect ratio of transistors in that error amplifier is designed to make the V_{OEA_MIN} equal to $\sim 0.1\text{V}$. The actual aspect ratio can be calculated using equation (6) shown in the following

$$\frac{W}{L} = \frac{I_Q}{\mu C_{OX} (V_{OEA_MIN})^2} \quad (6).$$

Channel length of power transistor is designed to be the minimum feature size of 0.13- μm CMOS technology (e.g. $L=0.13\mu\text{m}$). The aspect ratio of power transistor calculated by the "linear region" approach shown in Table I is adopted.

Fig. 5 shows the simulated open loop-gain response of LDO operated at three different current levels (e.g. 50mA, 5mA, and 500 μA) in which the r_{op} is small enough to make the pole P_{OLDO} far away from the unity-gain frequency. The phase margin (PM) at 50mA I_{LOAD} is ~ 100 degree, at 5mA I_{LOAD} is ~ 81 degree, and at 500 μA I_{LOAD} is ~ 71 degree. As the power transistor is designed to operate in linear region at the dropout condition, the loop gain is decreased from $\sim 46\text{dB}$ at 500 μA I_{LOAD} to $\sim 12\text{dB}$ at 50mA I_{LOAD} .

Fig. 6 shows the simulated open loop-gain response of LDO operated at another three different current levels (e.g. 50 μA , 10 μA , and 5 μA) in which the r_{op} increases rapidly such that the pole P_{OLDO} is moved toward the unity-gain frequency. The PM at 50 μA I_{LOAD} is ~ 63 degree. When I_{LOAD} is at 10 μA , the PM is decreased to ~ 32 degree. The PM at 5 μA I_{LOAD} is just ~ 2 degree that means the pole P_{OLDO} is at the f_{UG} .

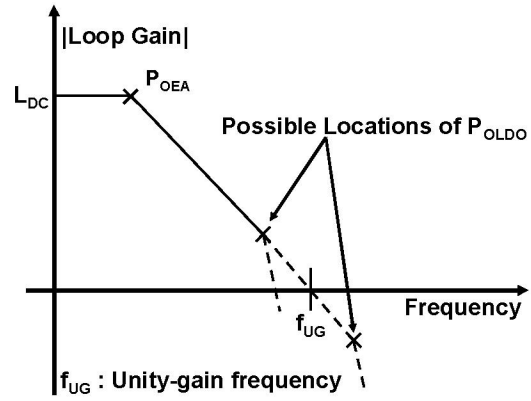


Fig. 3 Open loop-gain magnitude plot of LDO appeared in Fig. 1.

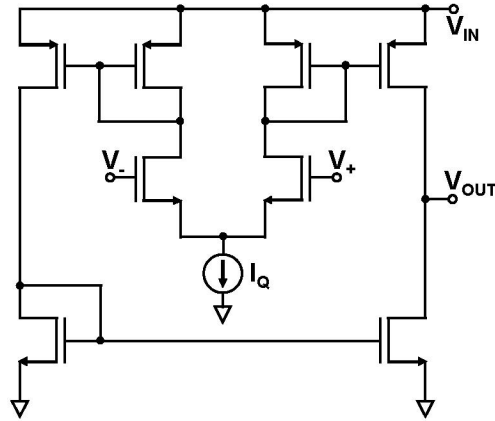


Fig. 4 Schematic of error amplifier used in LDO simulations.

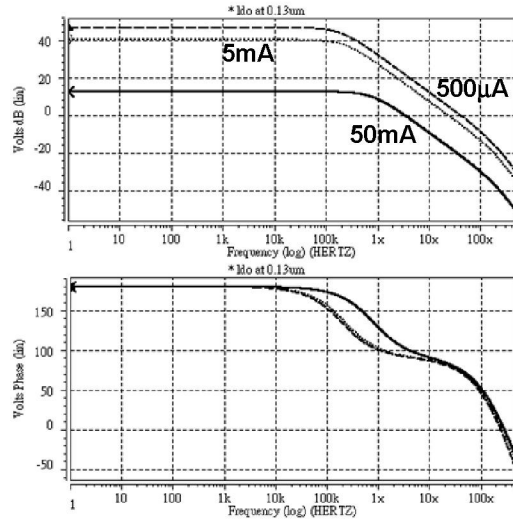


Fig. 5 Simulated open loop-gain response of LDO operated at three different current levels such as 50mA, 5mA and 500 μA .

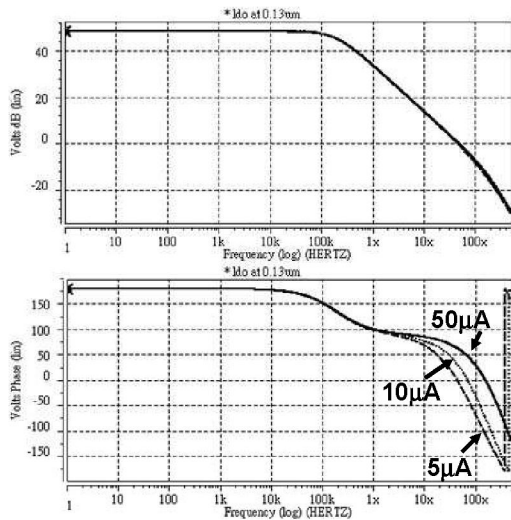


Fig. 6 Simulated open loop-gain response of LDO operated at another three different current levels such as $50\mu\text{A}$, $10\mu\text{A}$ and $5\mu\text{A}$.

IV. CONCLUSION

Design methodology of area-efficient and low-quiescent-current LDOs for chip-level power management is given in this paper. By designing the power transistor operated in linear region at the dropout condition, aspect ratio of power transistor is reduced by almost four times when compared to the power transistor designed to operate in saturation region. This significantly aspect ratio reduction helps to improve error amplifier slew-rate without increasing the quiescent current consumption. It is also found that stability of LDO designed under the proposed guideline has a minimum load

current requirement. According to the stability criterion derived in this work, the minimum load current requirement can be released by using a larger size power transistor.

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