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A Hybrid LED Driver with Improved Efficiency

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Abstract—A high-efficient hybrid light-emitting diode (LED) driver is introduced in this paper. By combining the merits of conventional switching-converter-based and inductor-less driving solutions, the proposed topology fully utilizes the input power from the AC mains without causing considerable switching loss or excessive voltage stress. With the help of a small-size inductor and the hybrid scheme, the proposed driver automatically alternates between switching mode and linear mode as the rectified input voltage changes. In addition, the driver can be configured either as a single stage for a high power factor (PF) and high efficiency or as the second stage of a two-stage solution for alleviating harmful low-frequency flicker. The proposed driver integrated circuit is implemented in a 0.35- μm high-voltage CMOS process and tested under 110-V_{AC} 60-Hz input. Measurement results show that, when operating in the high PF configuration, the proposed driver achieves 95.1% power efficiency and 0.986 PF. For the low flicker configuration, it achieves 92% efficiency and 15% flicker while maintaining a 0.918 PF.

Index Terms—Light-emitting diode (LED), AC-DC, high voltage LED driver, hybrid driver, flicker, inductance reduction and efficiency improvement.

I. INTRODUCTION

The breakthrough of high-brightness light-emitting diodes (LEDs) and the continuous decrease of the production and packaging cost over the past decade has led LED lamps to overwhelmingly dominate the general lighting market [1]. Despite the supreme efficacy of LED chips, to improve the energy-effectiveness for lighting, minimizing the electrical power losses from AC mains to the LED loads is essential. Thus, high efficiency is a primary but challenging demand for the design of LED drivers. Meanwhile, it is always desirable to accomplish efficient power delivery with a small form factor and a low hardware expense, which poses more challenges for the implementation of the driving circuits [2].

The inductive switching converter is one popular and straightforward approach to drive LEDs [3]–[14]. Fig. 1(a) illustrates a typical example of an inverted-buck converter,

which provides power to LEDs from the rectified high voltage node V_{IN} . Yet, as illustrated in the below equation, because of the high peak voltage of V_{IN} , the inductor L needs to have a large value to keep the same inductor current ripple of ΔI .

$$L = \frac{D \cdot (1-D) \cdot V_{IN}}{\Delta I \cdot f_S} \quad (1)$$

where D is the duty ratio and f_S is the switching frequency. Meanwhile, the parasitic elements introduced by the high-voltage components of the power stage have become a serious concern for the system efficiency. It is even worse if a higher switching frequency is adopted to reduce the volume of the inductor since the switching-dependent losses will increase to be unacceptably high. As a result, the switching frequency of the commercial switching-converter-based drivers is seldom pushed over the megahertz range and the inductors are typically several millihenry, which is relatively ineffective in terms of system volume and weight [3]–[5].

As illustrated in Fig. 1(a), the switching loss of the inverted-buck converter is majorly contributed by the drain parasitic capacitor C_{DS} of the power transistor M_1 . It has to be charged and discharged in each switching cycle with a large voltage swing, and the loss is given as

$$P_{SW,DS} = \frac{1}{2} \cdot C_{DS} \cdot V_{IN}^2 \cdot f_S \quad (2)$$

In addition, during the turn-on (turn-off) transition of M_1 , the drain-voltage V_{DS} (drain-current I_M) does not instantly fall to zero due to the gate parasitic capacitor C_{GD} and C_{GS} , resulting in crossover turn-on (turn-off) loss P_{ON} (P_{OFF}). Moreover, the minority carriers stored in the pn-junction of the power diode D limit its response speed during the turn-on of M_1 and cause negative current flow and reverse recovery loss P_{RR} . Both the crossover loss and the reverse recovery loss are proportional to the voltage swing and the switching frequency.

$$\{P_{ON}, P_{OFF}, P_{RR}\} \propto V_{IN} \cdot f_S \cdot \{t_{ON}, t_{OFF}, t_{RR}\} \quad (3)$$

where t_{ON} , t_{OFF} and t_{RR} are turn-on, turn-off and reverse recovery time, respectively, which are all determined by the parasitic capacitors in the power stage.

Aiming to reduce the switching-introduced losses, various techniques have been proposed. The emerging wide band-gap semiconductor devices, e.g. gallium nitride (GaN) based device, are promising to replace the conventional silicon power switches and diodes due to the significant decrease of parasitic capacitances [6]–[8]. However, these advanced devices currently show less reliability compared to their silicon counterparts and are still too expensive for general lighting applications. The switching losses can also be effectively minimized with the help of a resonant or quasi-resonant topology, in which an extra inductor is added to resonate with the parasitic drain capacitor [8]–[10]. Thus, the drain voltage falls to zero or near-zero before the turn-on switching to reduce

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Fig. 1. Conventional AC LED drivers based on (a) switching converter and (b) inductor-less linear topology.

V_{IN} . Nevertheless, the additional inductor also increases volume and weight, so the size reduction of the main inductor becomes less economically attractive. Also, the transistors in the resonant topology suffers from higher voltage stress, making it unfeasible to be monolithically integrated with the controller.

Fig. 1(b) illustrates an alternative switching-loss-free approach to drive the LEDs, namely, an inductor-less linear driver, which is particularly promising for integration since the magnetics are eliminated from the driver [15]–[20]. Instead of converting the varied high voltage V_{IN} to a stable low voltage for the loads, the LEDs are stacked and segmented to match the changes of V_{IN} . Therefore, the LED segments are switched on/off one by one as the input voltage increases/decreases. Taking the case of $(V_{LED1} + V_{LED2}) < V_{IN} < (V_{LED1} + V_{LED2} + V_{LED3})$ as a example, the active part of the inductor-less driver in the dashed-line box becomes a linear regulator. Then, the voltage difference between V_{IN} and $V_{LED1} + V_{LED2}$ will cause voltage drop and power dissipation on M_2 . Also, it is noticed that the quality of the power transistor has little impact on this unmatched-voltage introduced power loss.

Besides the consideration of efficiency, power factor (PF) and flicker are also important measures for AC-powered LED drivers [21]. However, high PF demands sine-wave like input power, while the low optical flicker requires constant LED power. This contradiction cannot be solved with a one-stage driver unless a bulky and unreliable electrolytic capacitor is adopted to filter the low frequency current ripple. Therefore, as illustrated in Fig. 2, one- or two-stage solution can be chosen for different lighting applications based on the acceptance of flicker [22]. The typical flicker produced by the AC LED lamps is located at the double line frequency (100 Hz or 120 Hz), which is invisible and considered less problematic for temporary illumination applications, such as lighting for corridors, roadways, and parking. In these cases, a one-stage solution with PF correction, which can be either a switching converter or an inductor-less driver, is adopted to minimize the cost and size while the flicker performance is sacrificed. In contrast, for most applications requiring visual concentration for the tasks of reading or watching, the two-stage solution in Fig. 2(b) is necessary to achieve a good PF and minimized flicker at the same time. As a result, efficiency and cost have to be sacrificed for two-stage drivers.

Fig. 2. (a) One-stage driver with high power factor and high efficiency. (b) Two-stage driver with low flicker.

In order to address the efficiency limitation of conventional switching-converter-based and inductor-less LED drivers, this paper introduces an AC-input hybrid driving solution with the merits of improved efficiency and reduced inductance [23]. The proposed driver can operate in either a high-PF configuration for the one-stage solution in Fig. 2(a) or a low flicker configuration as the second stage of the two-stage solution in Fig. 2(b).

The rest of this paper is organized as follows. The concept and benefits of the proposed hybrid driver will be introduced in Section II. Then, the architecture of the proposed driver for both the high-PF and low-flicker configurations, as well as the detailed implementation of the building blocks, will be given in Section III. Finally, the experimental results and conclusion will be presented in Section IV and V, respectively.

II. PROPOSED HYBRID DRIVER

A. Operation Concept

Here, the concept and analysis of the proposed hybrid driver

Fig. 3. Concept of the proposed hybrid LED driver with an example of a 3-segment LED string. (a) Simplified schematic. (b) Operation states. (c) State machine diagram. (d) Key waveforms.

with the high PF configuration will first be discussed, and in the last part of this section, we will extend the discussion to the low flicker configuration.

Illustrated in Fig. 3(a), the proposed design is the combination of the conventional switching converter and an inductor-less driver. Specifically, a small inductor is added in front of the LED string, different to the inductor-less topology in Fig. 1(b), in order to save the energy dissipated on the power transistors. The operation states, diagram of the state machine and key waveforms of the proposed driver are also illustrated in Fig. 3. For a certain input voltage V_{IN} , for example in state-2 ($V_{LED1} < V_{IN} \leq V_{LED1} + V_{LED2}$), only one power transistor M_1 can be switched on and off. Meanwhile, its right-hand adjacent transistor M_2 stays fully on in this state and the left power transistors remain off. It is noticed that the control scheme of the hybrid converter, as shown in Fig.3 (b), is slightly different from our last version design in [23], in which two power transistors need to be switched on and off in each state. We make this modification in the updated design because it is unnecessary to switch the second transistor off. In fact, there is no current flowing through the second path when the first path is activated regardless of the status of the second transistor. Then, a sensing resistor R_s is utilized to sense the inductor current I_L , and a hysteretic control scheme is used to ensure I_L is bounded inside the hysteretic window. When M_1 is on, the voltage difference of V_{IN} and $V_{LED1} + V_{LED2}$ drops on the inductor, and the extra energy is stored in the inductor by increasing I_L from I_{LO1} . Then, after I_L reaches a higher boundary I_{HI1} , M_1 will be switched off and the current will flow through M_2 . Despite V_{IN} being smaller than $V_{LED1} + V_{LED2}$, the two LED segments can still be lit up with the energy stored in the inductor until I_L falls to I_{LO1} again. Thus, the power loss caused by the mismatch of the input voltage and LED voltage in the inductor-less linear driver can be effectively saved.

Next, as V_{IN} approaches $V_{LED1} + V_{LED2}$, it takes a shorter time to charge and longer time to discharge the inductor. Eventually, when V_{IN} goes up to $V_{LED1} + V_{LED2}$, I_L is unable to reach the low boundary I_{LO1} . In this case, the hybrid driver operates just as the conventional inductor-less linear driver does, but with almost zero voltage as well as energy loss on the power transistor. Since V_{IN} rises relatively slowly, the driver stays in a linear mode for a long period until the LED current increases to I_{HI1} . It is noticed that the voltage across the inductor is almost zero in this period and there is no switching loss. Then, the double-hit of the high boundary triggers the transition to the next operation state (state-3), in which the above procedure will repeat.

Fig. 4. (a) Simplified schematic and inductor current waveform for state-K. (b) The switching frequency of the hybrid converter under different conditions.

Fig. 5. The power loss mechanisms for the proposed hybrid LED driver. (a) Diagram of inductor current. (b) Switching loss during turn-on procedure. (c) Switching loss during turn-off procedure. (d) Conduction loss.

As shown in Fig. 3(d), a group of hysteretic boundaries (I_{LOX} , I_{HIK}) are set for the different states for the high PF configuration with one-stage power conversion. This is done so that the envelope of the input current (LED current) will follow the shape of the input voltage. As a result, a high PF can be achieved. More importantly, the operation states decisions are fully automatic and do not demand sensing the high-voltage nodes, significantly reducing the controller's complexity.

It is noticed that Fig. 3 only shows the general concept of the proposed hybrid driver with an example of a 3-segment LED string. However, the idea is feasible to extend to the N-segment topology with more power transistors and operation states.

B. Analysis of Inductance Reduction

As previously mentioned, the inductor size of the switching-converter-based driver is limited by the maximum input voltage ($V_{IN,MAX}$) and the allowed peak frequency ($f_{S,MAX}$) for the same inductor current ripple (ΔI). The required inductance for the buck converter in Fig. 1(a) can be written as

$$L_{BUCK} = \frac{(1-D) \cdot V_{LED}}{\Delta I \cdot f_{S,MAX}} = \frac{1}{\Delta I \cdot f_{S,MAX}} \cdot \left(1 - \frac{V_{LED}}{V_{IN,MAX}}\right) \cdot V_{LED}. \quad (4)$$

In comparison, the required inductance can be effectively scaled down with the proposed hybrid topology. Fig. 4(a) shows the simplified circuit taking the state-k as an example. In this state, V_{IN} is larger than the sum of forward voltage of the first k-1 LED segments $V_{LED\SUM,K-1}$ but smaller than $V_{LED\SUM,K-1} + V_{LEDK}$. For the hysteretic control with a fixed current ripple, the maximum switching frequency happens when the charge period T_1 equals the discharge period T_2 , and the required inductance L_{HYB} can be written as

$$L_{HYB} = \frac{V_{LEDK}}{4 \cdot \Delta I \cdot f_{S,MAX}}. \quad (5)$$

Therefore, with an increase of the total LED segment number N , it is feasible to reduce the forward voltage of each segment V_{LEDK} as well as L_{HYB} . A more intuitive comparison of switching frequency versus V_{IN} between four conditions (with different typologies, inductance and segment numbers) under 110-V_{AC} input is given in Fig. 4(b). It clearly shows that the inductance of the hybrid driver with seven segments (condition4) is less than one tenth that of the conventional buck driver (condition1) for a comparable peak switching frequency. In addition, by comparing the three conditions with hybrid driving approach, it shows that the maximum switching frequency can be reduced by increasing the inductor value L and/or increasing the number of segments N . Condition4 is

chosen in this design for the balance of inductance and segment number.

C. Analysis of Power Loss

Besides the merit of inductance reduction, the proposed hybrid solution also shows significant improvement in terms of efficiency. The key is to reduce the voltage swings on the high-voltage switching nodes. Fig. 5 illustrates the main power loss mechanisms of the hybrid driver with the example of state-2 ($V_{LED1} < V_{IN} \leq V_{LED1} + V_{LED2}$). Power transistor M_1 is switched on and off in this state, so that the parasitic LED capacitor C_{LED2} and drain capacitor C_{DS1} become the main contributors to the switching loss, which can be written as

$$P_{SW,DS} = \frac{1}{2} (C_{LED2} + C_{DS1}) \cdot V_{LED2}^2 \cdot f_S. \quad (6)$$

Also, it is noticed that both C_{LED2} and C_{DS1} highly depend on their operation voltages, which is related to node voltage V_{D1} in Fig. 5.

Fig. 6. Simulated results for the high PF configuration with a 6.8- μ H inductor and seven segments of LEDs. (a) Efficiency versus input voltage. (b) Power breakdown versus input voltage. (c) Power breakdown for 110 V_{AC} input.

In addition, the turn-on and turn-off loss can be derived as

$$\{P_{ON}, P_{OFF}\} \propto V_{LED2} \cdot f_s \cdot \{t_{ON}, t_{OFF}\}. \quad (7)$$

Comparing equations (6) and (7) with (1) and (2), the switching voltage swing of the hybrid driver is alleviated from V_{IN} to V_{LED2} , thereby reducing the entire switching related losses. The efficiency is also benefited with a larger N due to the negative correlation of V_{LED2} (or V_{LEDK}) with N .

In addition, the added small inductor stores and releases energy in each cycle, so the power transistors can be fully switched on to minimize the voltage drop on the power stage. Then, the conduction loss, introduced by the parasitic resistors of the power inductor R_L , the power transistor R_{ON} and the sense resistor R_S , can be derived as

$$P_{COND} = (R_S + R_L + DR_{ON,M1} + (1-D)R_{ON,M2}) \cdot I_{L,RMS}^2 \quad (8)$$

where $I_{L,RMS}$ is the root mean square value of the inductor current.

Furthermore, the voltage drop on the full bridge rectifier (not shown in Fig. 5) also contributes to a large proportion of

the system power loss, which is given as P_{REC} .

The effectiveness of the loss reduction of the hybrid driver is verified with the simulated plots in Fig. 6. A 6.8- μ H inductor and seven segments of LEDs are utilized in the simulation, while the parasitic resistance R_L and parasitic capacitance C_{LED} are all extracted from the measured data and included in the simulation models. Besides this, the model of the on-chip high-voltage transistors, provided by the fabrication foundry, also includes the voltage-dependent capacitors C_{GD} and C_{DS} . As shown in Fig. 6(a) and (b), the input current as well as the input power increases with the input voltage for the high-PF configuration, and despite the over 5-MHz peak switching frequency, the efficiency is over 95% in most of the working range. The theoretical maximum achievable efficiency of the inductor-less driver with the same LED segments is also illustrated in Fig. 6(a) for comparison. Fig. 6(c) shows the simulated system power breakdown at 110-V_{AC} input, indicating a 97.8% achieved efficiency. It is noted that, besides the loss on the rectifier, only about 0.9% delivered energy is wasted on the power stage of the driver. Under the same condition, the simulated PF is 0.976.

D. Extension to Low Flicker Configuration

For applications requiring low flicker, the hybrid topology can be employed as the second stage of the configuration in Fig. 2(b). Fig. 7 shows the simplified schematic and waveform diagrams of this configuration, also with a 3-segment example.

The first stage is implemented with an off-chip passive valley-fill power factor correction (PFC) circuit to concurrently provide a good PF and to reduce the voltage ripple on V_{IN} . This is a rather simple PFC, suitable for low- to moderate-power LED systems [25], [26]. When the rectified line voltage approaches the peak, it is applied across C_1 and C_2 with a series connection, as they are both charged up to approximately half of the peak line voltage. A resistor inside the circuit is used to prevent a large in-rush current. When the line voltage falls below half of the peak voltage, C_1 and C_2 are set in parallel and begin to discharge into the second stage. For the rest of the line period, the circuit is disabled as there is no charge or discharge procedure.

For the low flicker configuration, the second stage needs to alleviate the impact of the large voltage ripple, which is over 50% of the peak voltage of V_{IN} , and obtain a light output with less fluctuation. This is achieved with a similar concept to that utilized in our previous design, in which we build a $1/x$ circuit in the driver and reconfigure the hysteretic boundaries (I_{LOX} , I_{HIX}) to be inversely proportional to V_{IN} [18], [19]. Thus, the product of the average LED current (the same as the average I_L) and the effective LED voltage (the same as the average V_{IN} and representing the number of enabled LEDs on the string) is kept almost constant in each cycle to reduce the low-frequency flicker. Also, the human eye naturally filters out the switching introduced high-frequency portion of the light output, which is not considered to be a health concern.

Fig. 8 shows the simulated power breakdown for the low flicker configuration at 110 V_{AC} input. In order to minimize the flicker, both the efficiency and PF are sacrificed in this case, while the hybrid topology can still achieve a competitive result, with 93.8% overall efficiency and a 0.91 PF.

Fig. 7. Extension to the low flicker configuration. (a) Simplified schematic. (b) Key waveforms.

Fig. 8. Simulated power breakdown of the proposed hybrid LED driver for low flicker configuration with a 6.8 μ H inductor and seven segments of LEDs.

Fig. 9. System architecture of the proposed hybrid LED driver.

III. CIRCUIT IMPLEMENTATION

A. System Architecture

The system architecture of the proposed hybrid LED driver is illustrated in Fig. 9. The driver can be set to operate either in the high PF or low flicker configuration with an external selection pin REF_SEL, while the off-chip valley-fill PFC is only necessary for the low flicker configuration (REF_SEL=1). Besides this, a small inductor is put between a full bridge rectifier and an LED string with seven segments. The LED current can flow through either one of the six on-chip power transistors (M_1 to M_6) or through the entire LED string. The power transistors are implemented with a 120V high-voltage NMOS in this design and their sizes are optimized and scale down from M_6 to M_1 for the high PF configuration. Meanwhile, it means that the sizes are not the best solution for the two-stage low flicker configuration.

Fig. 10. Reference boundaries generator for the high PF configuration.

Then, the current is converted to voltage V_S and fed back to the controller. It is noted that V_S cannot be directly compared with the reference boundaries V_{LO} and V_{HI} because the switching introduced spikes may cause unexpected state changes. Therefore, a blanking circuit is needed to suppress these spikes at each leading and falling edge of the switching signal. The boundaries are generated accordingly with separated blocks (high PF reference generator and $1/x$ circuit) for different configurations. After the comparison and a latch, the output signals R, S and Q are taken as the inputs of the state controller.

The different output combinations of the state controller (A_2 , A_1 and A_0) represent eight operation states (3-bit). As discussed in the last section, two adjacent power transistors (M_n and M_{n+1}) are enabled for each state, while the others are fully switched off. Then, M_n is controlled and switched by signal Q and M_{n+1} is kept on with low resistance. Therefore, the operation mechanisms shown in Fig. 3 and Fig. 7 can be successfully realized with the above system implementation.

B. Reference Boundaries Generator

Fig. 10 illustrates the reference boundary voltage generator for the high PF configuration, in which the outputs V_{HI} and V_{LO} go up with the 3-bit operation state ($A_2A_1A_0$). V_{R1} is provided externally for the sake of flexibility of debugging/tuning and typically set to 300mV in this design, and other reference voltages are generated from V_{R1} with a resistor divider. A 3-8 decoder converts $A_2A_1A_0$ to an 8-bit signal (state-7 to state-0) and uses it to select the voltage for the two boundaries. The hysteretic window set by the voltage difference of V_{HI1} and V_{LO1} is kept as one third of V_{R1} .

Fig. 11 shows the schematic and key waveforms of the $1/x$ circuit, which is utilized to generate the reference boundaries for the low flicker configuration [19], [27]. The circuit can be divided into three parts. In the first part (V-I conversion), the scaled input voltage V_{IN_IN} (equals $V_{IN}/111$ in this design) and a reference voltage V_{REF2} are converted into currents I_{IN} and I_{REF2} , respectively. In the second part (core process), two matched capacitors, C_1 and C_2 , are fully discharged, with a reset signal RS_{IOX} . Then, I_{IN} and I_{REF2} are used to charge these two capacitors until the voltage on C_1 reaches another reference voltage V_{REF1} . For the same charging period, as shown in Fig. 11(a), the voltage held on C_2 can be derived as

$$V_{C2} = \frac{V_{REF1} \times I_{REF2}}{I_{IN}} = \frac{V_{REF1} \times V_{REF2}}{V_{IN_IN}} \quad (9)$$

which is inversely proportional to V_{IN_IN} as well as V_{IN} . The last part (output stage), composed of sample and hold circuits, analog buffers and resistor dividers, is employed to keep the obtained V_{C2} and to provide the final reference voltages.

In order to improve the accuracy of the $1/x$ circuit, the current mirror of the V-I converter, as shown in Fig. 11(b), are swapped during each reset period. Meanwhile, the output stage samples V_{C2} in two phases (Φ_1 and Φ_2) separately and averages these two sampled voltages to obtain V_{HI2} and V_{LO2} .

The detailed implementation of the signal generator in Fig. 11 has been discussed in our previous design [19]. We utilize almost the same circuit here except that an off-chip clock is used for testing flexibility.

Fig. 11. Reference boundaries generator for the low flicker configuration. (a) 1/x circuit. (b) V-I converter. (c) Diagram of the key waveforms.

C. Comparator and Digital Controller

Fig. 12 shows the schematic of the main comparator in the proposed driver. A peaking current source circuit is used to provide a built-in bias current that is insensitive to variation of the power supply voltage. Then, three stages are employed to accomplish the comparison. In the decision stage, M_{P5} to M_{P9} form a cross coupled circuit and the size of M_{P5} and M_{P8} is set to be larger than M_{P6} and M_{P7} . Thus, hysteresis is added in the comparator to enhance its immunity to noise.

Fig. 13 shows the schematic of the digital controller as well as the diagrams of the main signals. The pulse of R (S) happens when the inductor current reaches the upper (lower) boundary. Then, as shown in Fig. 13, the alternate pulses of R and S

Fig. 12. Comparator in the proposed hybrid driver.

Fig. 13. Digital controller in the proposed hybrid driver. (a) Schematic. (b) Diagram of key waveforms.

Fig. 14. Chip micrograph of the proposed hybrid driver IC.

Fig. 15. PCB and test setup for the proposed hybrid driver IC. (a) LED and inductor board. (b) Driver board. (c) Valley-Fill circuit board. (d) Test setup for high PF configuration. (e) Test setup for low flicker configuration.

Fig. 16. Measured plots of 1/x circuit.

Fig. 17. Measured waveforms for the high PF configuration at different input voltages. (a) 110 V_{AC}. (b) 100 V_{AC}. (c) 120 V_{AC}.

Fig. 18. Measured waveforms for the low flicker configuration at different input voltages. (a) 110 V_{AC}. (b) 100 V_{AC}. (c) 120 V_{AC}.

maintain the current operation state ($A_2A_1A_0$), while the successive pulses trigger the 3-bit up-down counter, resulting in state change. Specifically, a double-pulse R adds “1” to the current state and a double-pulse S subtracts “1” from the current state. Finally, $A_2A_1A_0$ and Q are translated to gate driving signals for controlling the power transistors.

Fig. 19. Measured results. (a) PF and efficiency for the high PF configuration. (b) PF and efficiency for the low flicker configuration. (c) Percent flicker for the low flicker configuration.

IV. MEASUREMENT RESULTS

The driver IC with the proposed hybrid control scheme was fabricated in a 0.35- μm 120-V CMOS process. Fig. 14 shows the chip micrograph, which measures 3.0 mm $\times$ 0.84 mm, including the controller and six integrated power transistors. Fig. 15 shows the PCB boards and setup for measuring the proposed driver IC.

As shown in Fig. 15 (a), a compact 6.8- μH inductor with a size of 3 mm $\times$ 3 mm $\times$ 1.3 mm is put close to the LED string [28]. The LED string is implemented with seven segments of high-voltage LEDs [29]. The forward LED voltage for the first segment is around 54 V (six of 9-V LEDs), while for the second to the last segment, the forward voltage is 18 V (each of 18-V LED). Besides the driver chip and rectifier, most of the components and area on the driver board in Fig. 15(b) are implemented for the testing purpose. Its size can be significantly reduced. The chip is designed and tested for both the high PF (Fig. 15(d)) and low flicker (Fig. 15(e)) applications with 110-V_{AC} input, though the concept of hybrid driver is also applicable to higher voltage applications with a suitable process. Besides this, an external 5-V voltage supply is used in the testing for powering the controller blocks, which can be replaced by a on-chip regulator. As discussed above and shown in Fig. 15 (c) and (e), in the low flicker configuration, the valley-fill circuit is needed as the PFC stage. In this prototype, it is composed of three off-chip diodes and four 10- μF high-voltage film capacitors as the energy buffer (C_1 and C_2 in Fig. 9).

Fig. 16 shows the measured plots of the $1/x$ circuit, indicating that its outputs V_{HI2} and V_{LO2} go in the opposite direction from input V_{IN_IN} (V_{IN}) just as expected. The gain accuracy in most of the working range is below 1%, and the worst case ($V_{IN_IN} = 0.4$ V) is also below 3%.

Fig. 17 and Fig. 18 show the measured waveforms of V_{IN} , V_X and I_L as well as the operation states $A_2A_1A_0$ at different AC input for the high PF and low flicker configuration, respectively. In both cases, V_X switches above and below V_{IN} with a voltage swing less than 20 V, which helps to significantly reduce the switching related loss. The zoomed-in waveforms also indicate that the maximum switching frequency is up to 5 MHz. For the

high PF configuration, the shape of I_L follows V_{IN} to achieve a good PF. By contrast, the envelope of I_L in Fig. 18 goes inversely to V_{IN} for achieving low flicker. A photo diode testing board is used to measure the percent flicker from the filtered light output V_{LO_LF} because only low-frequency flicker (< 3 -kHz) has potential health concerns [22].

The measured power efficiency, PF and percent flicker for two configurations are illustrated in Fig. 19. For each configuration, two power level cases are measured and plotted under 100–120 V_{AC} (20W/10W for high PF configuration in Fig. 19(a), and 15W/10W for high PF configuration in Fig. 19 (b) and (c)). The results show that the proposed hybrid design can operate in either configuration, and just as expected, the high PF configuration achieves better performance in terms of PF and efficiency while the low flicker configuration is featured with reduced flicker. Table I summarizes and compares the performance of this design with prior-art AC-input LED drivers, indicating that the hybrid scheme improves the system efficiency for both cases even with less number of LED segments. More importantly, it is achieved by only adding a compact 6.8-μH inductor, which is effective in terms of system cost and volume.

V. CONCLUSION

A hybrid control scheme is introduced in this paper in order to achieve inductance reduction and efficiency improvement for an AC-input LED driver. Depending on the lighting application, the proposed design is capable of operating in either a high PF or low flicker configuration. In addition, it fully utilizes the input power, with a small inductor to store and

release energy, and greatly reduces the voltage swing on the switching nodes to minimize the switching related losses. The proposed driver is demonstrated with a prototype chip, which is designed and fabricated in a 0.35-μm high-voltage CMOS process. The measurement results show that, by using only a 6.8-μH inductor, the hybrid driver achieves 95.1% power efficiency and a 0.986 PF for the high PF configuration, and 97% power efficiency, 15% flicker and a 0.918 PF for the low flicker configuration.

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Table I Performance Comparison with State-of-the-Art AC-input LED Drivers.

	ISSCC2013 [6]	JSSC2012 [9]	TPEL2012 [30]	ISSCC2013 [12]	ISSCC2016 [14]	JSSC2018 [16]	This Work	
Stage	Single	Single	Two	Single	Single	Two	Single	Two
Driver Type	Buck Resonant Switching Converter	Fly-back Switching Converter	Fly-back & Buck/Boost Switching Converter	Inductor-Less Linear	Inductor-Less Linear	Valley-Fill PFC & Inductor-Less Linear	Hybrid	Valley-Fill PFC & Hybrid
Process	0.35-μm CMOS	0.35-μm BCDMOS	Discrete Components	1-μm 450V BCDMOS	0.18-μm 85V BCDMOS	0.35-μm 120V CMOS	0.35-μm 120V CMOS	
Chip Area	22.1 mm ²	0.75 mm ²	-	9.64 mm ²	0.77 × 3 mm ²	4.2 mm ²	2.52 mm ²	
LED Segment	1	1	1	6	6	12	7	
Power Switch	Off-chip (GaN)	Off-chip	Off-chip	On-chip	On-chip	On-chip	On-chip	
Magnetics	Inductors (850 nH & 12 μH)	Transformer (1.8 mH)	Transformer (80 μH) Inductors (500 μH & 30 μH)	No	No	No	6.8 μH	
Max. Switching Frequency	11 MHz	~ 110 kHz*	200 kHz & 100 kHz	No	No	No	~ 5 MHz	
Max. Power	22 W	12 W	33.6 W	22 W	34 W	8 W	20 W	15 W
Input Voltage	110 V _{AC}	180-260 V _{AC}	90-264 V _{AC}	110/220 V _{AC}	120 V _{AC}	110 V _{AC}	110 V _{AC}	
Power Factor	0.96	0.96	> 0.99*	0.99	0.996	0.904	0.986	0.918
Percent Flicker	~ 100 %*	~ 30 %*	< 3 %*	~ 100 %*	~ 100 %*	6.4 %*	100 %	15.4 %
Peak Efficiency	89.5 %	85 %	85.5 %	92.2/93.4 %	83 %	89.2 %	95.1 %	92 %

* Not reported in the paper. Estimated from the measured waveforms.

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