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An 8-nW Resistor-less Bandgap Reference Based on a Single-Branch Floating PTAT Voltage

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Abstract—This letter presents an ultra-low-power resistor-less bandgap reference circuit, which is based on the topology of a single-branch floating PTAT voltage. By using a cascode high impedance current bias technique, the single-branch PTAT voltage can be directly floating on the CTAT voltage generated by the V_{EB} of the bipolar transistor. Ultra-low power consumption is realized by the simple topology in the proposed method, which only needs a few current branches. Fabricated in 0.13- μm CMOS process, this work generates a 1.252-V bandgap reference voltage. The total power consumption is 8.26 nW with a 1.4-V supply voltage. Without a resistor, this work can achieve a small active area of 0.017 mm^2 . The average value of the temperature coefficient is 68 ppm/ $^{\circ}\text{C}$ from -20°C to 110°C , and the line regulation is 0.019 %/V.

Index Terms—Bandgap reference, low-power, resistor-less, nano-watt, floating PTAT voltage.

I. INTRODUCTION

Ultra-low-power voltage references have been given more attention in recent research since they are a necessary building block in low-power internet of things (IoT) systems. In most voltage references, resistors are a common choice to generate proportional-to-absolute-temperature (PTAT) current and PTAT voltage. To suppress the resistor current, large resistors are used to achieve low-power consumption, which will consume a large chip area [1]. The CMOS-only topology becomes a popular choice to achieve an ultra-low power voltage reference while consuming only a small active area [2]. However, in the CMOS-only method, the output voltage accuracy is degraded by process variation since the reference voltage is strongly dependent on threshold voltage. Therefore, the bipolar-junction-transistor (BJT)-based bandgap reference with ultra-low power consumption is indispensable for the low power system, which needs a high accuracy reference voltage. Switching capacitor topology can be used to divide the emitter to the base voltage (V_{EB}) of the BJT and reduce the supply voltage overhead in the bandgap reference [3], [4]. However, the switching noise generated by the switching capacitor will be coupled to the system. Differential pairs can be used to generate a floating PTAT voltage based on the differential voltage between V_{GS} of transistors in the subthreshold region [5]–[8]. However, many differential pairs are needed to generate an adequate PTAT voltage, which will induce large current consumption. In [9], a leakage-current-based bandgap reference that can operate under nano-watt power is proposed. However, a mega-ohm level resistor is still needed to achieve nano-amp current consumption. A trimming network for the resistor is also needed to get the desired current consumption and accurate temperature-independent reference voltage since the

fabricated poly-resistor will have a huge deviation from the designed resistance value due to the process variation from implantation and poly film deposition.

In this paper, a resistor-less topology of an ultra-low-power bandgap reference is proposed. In order to avoid using resistors to combine complementary-to-absolute-temperature (CTAT) voltage and PTAT voltage in the bandgap reference, a floating PTAT voltage is realized based on the leakage current of the transistor in the subthreshold region with cascode high impedance current bias. The CTAT voltage is generated by the V_{EB} of the bipolar transistor, which is biased by a resistor-less current source.

II. PROPOSED BANDGAP REFERENCE CIRCUIT

A. Core Bandgap Reference Circuit

Fig. 1. Topology of proposed bandgap reference circuit.

The proposed bandgap reference circuit is shown in Fig. 1. VDD1, VDD2 and VDD_BF are biased by the same voltage with different pads on the chip. The separation is used to test the current consumption of different parts in the circuit. VDD1 is used to bias the current source and BJT branch. VDD2 is used to bias the PTAT voltage generator. VDD_BF biases the supply voltage of the on-chip buffer. The core bandgap circuit consists of two parts: the CTAT voltage and the PTAT

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voltage generator. The CTAT voltage is generated by a PNP bipolar transistor biased with a threshold voltage independent current source, which will be explained in detail in Section II C. The emitter area of the PNP device is $25 \mu\text{m}^2$. The floating PTAT voltage is generated by flowing the leakage current generated by a zero- V_{GS} PMOS M09 into series diode-connected PMOS M08s. The P-MOSFET saturation current in the subthreshold region is shown in (1) [10],

$$I_{sd} = \mu_p C_{ox} \left(\frac{W}{L} \right) (\eta - 1) V_T^2 \exp \left(\frac{|V_{gs}| - |V_{thp}|}{\eta V_T} \right). \quad (1)$$

By assuming that the threshold voltage of M08 and M09 is the same for the same transistor finger size, the source to gate voltage of M08 can be expressed as

$$V_{sg,M08} = \eta V_T \ln \left(\frac{W_{M09} L_{M08}}{W_{M08} L_{M09}} \right), \quad (2)$$

where μ_p , C_{ox} , W , L , η , V_T and V_{thp} is the hole mobility, the gate oxide capacitance per area, the transistor total channel width, the transistor finger length, the inverse of gate-to-surface coupling coefficient, the thermal voltage and the P-MOSFET threshold voltage, respectively. In this work, six PMOS M08 in series are used to compensate the temperature slope of the CTAT voltage from the BJT. Thus, the reference output voltage is given by

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{CTAT} + 6 \cdot V_{sg,M08}. \quad (3)$$

To realize the addition of CTAT and PTAT voltage without a resistor, the PTAT voltage should be floating while maintaining a decent temperature coefficient and line regulation. The drain current of M08 should equal the drain current of M09 in all possible CTAT voltage DC conditions over a large temperature range. For the floating PTAT voltage branch, the top current ($I_{sd,M05}$) and the bottom current ($I_{ds,M10}$) which are biased by the drain current of M09 should be the same over a large temperature range, otherwise an error-current (I_{EC}) will flow into the BJT as shown in Fig. 1. A large I_{EC} has major impact on the performance of the temperature coefficient since I_{EC} is strongly threshold voltage dependent. I_{EC} can be expressed as

$$I_{EC} = K \cdot I_{sd,M09} = K \mu_p C_{ox} \left(\frac{W_{M09}}{L_{M09}} \right) (\eta - 1) V_T^2 \exp \left(\frac{-|V_{thp}|}{\eta V_T} \right), \quad (4)$$

where K is the mismatch ratio. It is clear that when I_{EC} flows to the emitter of the BJT, the threshold voltage variation will be coupled to the CTAT voltage and the temperature slope. This coupling will eventually degrade the reference voltage accuracy and temperature coefficient.

In order to achieve a decent temperature coefficient, the CTAT voltage ranging over the temperature consideration is necessary. Thus, I_{EC} should be minimized for the accuracy of the reference voltage. The cascode current mirror topology must be used to minimize I_{EC} . Fig. 2 shows the comparison of the simulated I_{EC} over temperature between the NMOS current mirror design of a non-cascode design scenario and the proposed cascode design scenario. Without using the cascode topology in the NMOS current mirror, the I_{EC} will be large especially at high temperature as shown in Fig. 2, since the $|V_{thp}|$ will decrease significantly with increasing temperature based on (4). If using the traditional cascode current mirror topology (as M01-M06) in the NMOS current mirror, the subthreshold saturation condition ($V_{DS} > 3V_T$) for NMOS cascode current mirror M10 is impossible to achieve at high temperature. Since the CTAT voltage will linearly decrease with a rising temperature. Thus, a cascode topology with high swing must be used in the NMOS current mirror. As shown in Fig. 1, a high swing cascode topology implemented by high- V_{TH} transistors (M12 & M13) and normal- V_{TH} transistors (M10 & M11) is used. The gate of M10 is directly biased by the V_{GS} of M12. The minimum voltage at M10's drain is $V_{GS,M12} - V_{GS,M10} + V_{DS,M10} = \Delta V_{GS} + 3V_T$. In this way, the saturation range of M10 is much relieved. From the simulation results shown in Fig. 2, by using the NMOS current mirror with the proposed cascode scenario, the I_{EC} is much smaller than that from the

topology without using the cascode scenario. Especially at high temperature, the difference in I_{EC} between these two scenarios is more obvious.

Fig. 2. Simulated I_{EC} over temperature comparison between the NMOS current mirror with non-cascode scenario and the NMOS current mirror.

Even the cascode structure is used in the PMOS and NMOS current mirrors. There is still minor mismatch in the drain current of PMOS M09 and M08. This problem will not impact the final results for reference voltage level and temperature coefficient. The mismatched current from M09 to M08 can be equivalent to the mismatch of the width of M09 (W_{M09}). Based on equation (2), with proper trimming code, the value of W_{M09} can be trimmed to get the desired PTAT voltage ($V_{sg,M08}$).

To achieve a decent line regulation, the total impedance in series of each branch should be high. For the branch of M06, the output impedance of M06 is boosted by the output impedance of M03. For the branch of M05, the output impedance of M05 is boosted by the output impedance of M02. These two branches are already high impedance paths. For the PMOS M09 current branch, M01, M04 and M09 are all in diode connection which output impedances are low. To relieve this problem, NMOS M07 is added to significantly reduce the gain from power supply to the drain current of M09. Thus, the leakage current generated by M09 is supply voltage independent, which makes the PTAT voltage independent of the supply voltage. In addition, the cascode structure is used in the current source to improve the line regulation of the current bias for BJT. The schematic of the current source is shown in Fig. 5 in Section II C. Thus, the reference voltage is immune to power supply voltage change.

The impedance seen at M10's drain is $789.5 \text{ M}\Omega$ based on simulation. The emitter voltage of BJT (V_{EB}) changes with temperature which can be considered as the voltage biasing for M10's drain. Since the impedance seen at M10's drain is very large, the error current I_{EC} can be very small. The gate of M07 is biased by the reference voltage. Thus, a positive feedback loop is formed without stability issue since the loop gain is much smaller than unity. The loop can be explained as: the increment of V_{REF1} will increase the drain current of M09 by the source degeneration topology of M07, the increased drain current of M09 is mirrored to M08 and causes the increment of PTAT voltage which will increase the V_{REF1} .

Since the branch current of V_{REF1} is very small at low temperature, which may have a chance of being disturbed by any PCB leakage current, a source-follower as shown in Fig. 1 is used as an on-chip buffer to test the reference voltage with a large temperature range. An isolated P-well NMOS is used in the buffer to eliminate the body effect. Thus, the output of the buffer V_{REF2} is a perfect half of V_{REF1} . The power consumption of the on-chip buffer is not considered in the total power consumption of this work. In the circuit system application, the BGR output V_{REF1} can directly drive a later stage such as a voltage regulator. Capacitor C1, C2 and Cout with 900fF value are implemented to stable the supply voltage and output voltage. Also the bandwidth is limited by the capacitance to provide a reduced total thermal noise power. The variation of the reference voltage V_{REF2} from Monte-Carlo simulation

is shown in Fig. 3. σ/μ is 2.49%.

Fig. 3. Monte-Carlo simulation results of reference voltage (100 samples).

B. Trimming Network

Fig. 4. Trimming network of M09 in the proposed bandgap reference.

The trimming network is applied to PMOS transistor M09 in the bandgap reference circuit, as shown in Fig. 4. The gate voltages of the PMOS transistors in M09 are controlled to be connected with a Vtrim node in the circuit or the supply voltage. When the gate voltage of M09 is connected to VDD2, the PMOS transistor is fully turned off. Thus, the transistor width of M09 can be trimmed for a decent temperature coefficient.

C. Current Source

Fig. 5. Current source structure.

The resistor-less current source structure with start-up circuit used in this work is shown in Fig. 5 [10]. Transistor M18 works in the linear region operating as a resistor. Except for M18, all the other transistors are operating in the subthreshold region. The threshold voltage in three pairs of transistors (M18, M27), (M19, M20) and (M28, M29) can cancel each other by using the same finger size in each pair. The output current of the current source is then independent of the transistor threshold voltage and can be tolerant of process variation. The output current of the current source is designed to be 1 nA, which is used as the current bias for the BJT. A cascode structure is used in the current source to improve the line regulation. The start-up circuit is implemented with a capacitor C_3 stacked on M17. The voltage across on the capacitor cannot change instantly. When the circuit is powered up, M16 will be turned on because of the pulled-up voltage from the capacitor, and the drain-to-source current of M16 will turn on the current source. In the steady state when the current source is fully powered-on, the current through M17 will pull the gate voltage of M16 to GND and the leakage current in the off-state is negligible for the turned-off transistor M16 with body effect.

III. MEASUREMENT RESULTS

The proposed bandgap reference was fabricated in a 0.13- μm CMOS process. The chip photo is shown in Fig. 6. In the fabrication, the chip was covered by dummy metal layers to meet the metal density rules. The layout shown in Fig. 6 is used to mark the location of each building block in the design. The active area is 0.017 mm^2 . V_{REF2} was used to test the temperature coefficient (TC). The buffer output V_{REF2} is half the value of V_{REF1} . In Fig. 7 (a) and (c), the untrimmed and trimmed reference voltage V_{REF2} from -20°C to 110°C is shown based on the testing results of 12 samples. When testing the distribution and line regulation of the reference voltage at room temperature, as shown in Figs. 7 (b) (d) and 8 (a), V_{REF1} was measured directly. Before trimming, σ/μ is 1.78%. After trimming, σ/μ is 1.03%, and the average value of V_{REF1} is 1.252 V. In Fig. 8 (a), when the supply voltage is changing from 1.4 V to 2 V, the average line regulation of the 12 samples is 0.0189 %/V. With the supply voltage changing from 1.4 V to 3.3 V, the average line regulation is 0.0599 %/V. In Fig. 8 (b), the noise measurement result of output voltage is shown with frequency from 10 Hz to 1 MHz. The noise is 6×10^{-6} V/ $\sqrt{\text{Hz}}$ at 10Hz. During the measurement, the output voltage V_{REF2} is connected with the spectrum analyzer through an LNA and a RC high-pass filter. The noise of the LNA is much smaller than the bandgap reference circuit, which will not influence the measurement result.

Fig. 6. Chip micrograph.

Fig. 7. Measured reference voltage with 12 sample chips. (a) Untrimmed BGR vs temperature. (b) Untrimmed distribution at room temperature. (c) Trimmed BGR vs temperature. (d) Trimmed distribution at room temperature.

Fig. 8. (a) Measurement results of line regulation from 12 samples. (b) Noise measurement result.

The TC value of each chip from -20°C to 110°C ranges from 44.9 ppm/ $^\circ\text{C}$ to 95.4 ppm/ $^\circ\text{C}$, which is given in Fig. 9 (a). The average TC value is 68 ppm/ $^\circ\text{C}$. Fig. 9 (b) shows the total current consumption with 1.4-V supply voltage at

room temperature of each sample chip. The average value of the total current consumption is 5.9 nA and the average total power consumption is 8.26 nW.

Fig. 9. (a) Temperature coefficient value of each sample chip. (b) Total current consumption at room temperature of each sample chip.

Fig. 10 shows the current consumption of the current source and CTAT current bias (I_{CS}) from VDD1, the current consumption of the PTAT voltage generator (I_{PTAT}) from VDD2, and the total current consumption (I_{TOTAL}) from (VDD1+VDD2) as a function of temperature from -20 °C to 110 °C with a 1.4-V supply voltage. The testing results are from one sample chip. The current consumption from the current source increases linearly with temperature [10]. The current consumption of the PTAT voltage generator increases exponentially with temperature. As shown in equation (1), when $V_{GS} = 0$, ' $-|V_{thp}|$ ' is the exponent of Euler's number 'e'. When the temperature increases, $|V_{thp}|$ will decrease and cause the source-drain current of M09 to increase exponentially. The total current consumption is dominated by the I_{CS} at low temperature and is dominated by the I_{PTAT} at high temperature. With a 1.4-V supply voltage, the total power consumption of this work is 6.04 nW at -20 °C, 8.21 nW at 30 °C, 37.5 nW at 100 °C and 51.7 nW at 110 °C, and thus this work can achieve low power consumption with a large temperature range. The comparison table is shown in Table I. Compared with other recent ultra-low-power bandgap reference designs, this work can achieve very low power consumption with a

very small chip area. The proposed bandgap reference topology can operate in a large temperature range from -20°C to 110°C, with a decent temperature coefficient. The line regulation is extremely small compared with other works since high impedance topology is implemented in each current branch in this work.

Fig. 10. Current consumption versus temperature.

IV. CONCLUSIONS

In this paper, a proposed resistor-less bandgap reference based on the topology of a single-branch floating PTAT voltage is presented. The CTAT voltage is generated by the V_{EB} of the BJT, which is biased by the current source. The PTAT voltage is generated by flowing the leakage current generated by a zero- V_{GS} PMOS M09 into series diode-connected PMOS M08s. With high impedance current biases, the PTAT voltage can be added to the CTAT voltage without using resistors. The proposed topology can achieve an ultra-low power consumption, which is 8.26 nW at 1.4-V supply voltage, and a small chip area of 0.017 mm². The average value of the reference voltage is 1.252 V and the average temperature coefficient is 68 ppm/°C from -20°C to 110°C.

TABLE I
PERFORMANCE COMPARISON

	This work	[5] 2020	[13] 2017	[9] 2017	[3] 2017	[4] 2015	[1] 2015	[6] 2013	[11] 2012	[12] 2010
Process (μm)	0.13	0.35	0.18	0.18	0.18	0.13	0.35	0.18	0.13	0.35
Type	BJT	BJT	CMOS	BJT	BJT	BJT	BJT	BJT	BJT	BJT
Vref (V)	1.252	1.17	1.25	1.238	0.24	0.498	1.176	1.09	0.256	1.18
Power (nW)	8.26	54	0.024	9.3	40	32	28.7	100	170	108
TC (ppm/°C)	68	65	11-73	26	58	75	13	147	40	215
Temperature range	-20°C- 110°C	0°C- 80°C	0°C- 100°C	0°C- 110°C	-25°C- 85°C	0°C- 80°C	-10°C- 110°C	-40°C- 120°C	-20°C- 85°C	-20°C- 80°C
Line Reg. (%/V)	0.019	0.112	0.31	0.08	0.46	2	0.198	N/A	N/A	0.45
σ/μ (%)	1.03	1.21	0.27	0.43	0.29	N/A	0.2	0.74	0.17	1.63
Noise at 10Hz (μV/sqr(Hz))	6	N/A	4	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Active Area (mm ²)	0.017	0.042	0.0025	0.055	0.058	0.026	0.48	0.029	0.07	0.21

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