Characterization of buried nitride silicon-on-insulator substrate

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Abstract. Buried nitride silicon-on-insulator (soi) substrates prepared using stationary beam synthesis have been characterized. It is found that surface Si layers and alpha and beta-phase silicon nitride layers of good quality can be formed in the soi structure if the implant and annealing conditions are suitably controlled. However, the high nitrogen content inside the surface Si layer has been found to create new problems to the direct fabrication of devices on the soi substrate.

1. Introduction

Silicon-on-insulator (SOI) substrate [1] is well recognized as a promising candidate for a variety of novel semiconductor applications such as ULSI, high voltage devices and 3D integration. Buried insulator [2] is one of the favourite techniques to produce SOI and there are already commercial products in buried oxide SOI. Compared with buried oxide, buried nitride has several advantages, for instance, the process is more economical and safer, and silicon nitride is a more stable insulator for low diffusivity impurities. On the other hand, the nitride also has several disadvantages such as non-stoichiometry, the nitrogen atoms that remain in the residual silicon (Si) and the leakage of current. In this work, we present results on the characterization and optimization study of buried nitride SOI substrates formed by implanting nitrogen into Si using a stationary beam and under cyclic implant temperatures. Such a synthesis method is used as it can provide more information on the dependence of nitride SOI formation upon different wafer temperatures during implantation.

2. Experimental details

The substrates used were $\langle 100 \rangle$, 1–2 Ω cm, 50 mm diameter p-type Wacker Si wafers. The wafers were chemically cleaned and were implanted with N^+ atoms at an energy of 150 keV and doses of 20–100% 1.2×10^{18} cm^{-2} using the Extrion 200–1000. Stationary beam currents of 0.05–0.4 mA and wafer scanning frequencies of about 0.008–0.3 s^{-1} were used. Implanted wafers were subsequently annealed at 1200–1300 $^{\circ}\text{C}$ for 2–10 h under a nitrogen flow. Samples of about 5×5 mm^2 were then cut

from the central portion of the nitrogen-implanted wafer and were characterized by the infrared (IR) absorption, x-ray diffraction, ellipsometry, electrical measurements, optical and scanning electron microscopy (OM and SEM), cross section transmission electron microscopy (XTEM) and Rutherford backscattering spectroscopy (RBS). The feasibility of fabricating devices on this new SOI substrate (without using epitaxy) has also been tested using a commercial 2 μm NMOS TFT technology.

3. Results and discussion

The dependence of the surface Si layer crystal quality on the processing conditions is shown in table 1. We found that despite severe temperature cycling due to different beam current and wafer scanning during implantation, buried nitride SOI substrates with residual Si layers of very good crystal quality ($< 10^4$ dislocations cm^{-2}) can still be formed provided the average and peak *in situ* wafer heating during implantation is sufficiently high (samples B, D, F). When the wafer temperature is low, the surface Si layer is highly defective ($> 10^7$ dislocations cm^{-2}) (samples A, C, E).

It is well known that the wafer temperature during implantation should be kept high (usually 500 $^{\circ}\text{C}$) in order to achieve a good quality single Si surface layer. Our results show that these constraints can be relaxed. Moreover, the low dislocation density of our crystal surface Si is highly comparable to the best reported results [5] prepared under similar conditions.

The dependence of nitride phase formation on the processing conditions is shown in table 2. We observed that both alpha- and beta-phase silicon nitride can be formed in the buried nitride layers under different beam current, wafer scanning and annealing conditions. While

Table 1. Crystallinity of surface silicon layers.

Samples ^a	Wafer scanning ^b (cm s ⁻¹), Beam current ^c (mA)	$T_{\max}$ — T_{av} — $T_{\min}$ (°C)	Dislocation density (cm ²)
A	0.0086, 0.15	610—330—100	> 10 ⁷
B	0.0086, 0.2	760—410—130	< 10 ⁴
C	0.086, 0.18	640—380—190	> 10 ⁷
D	0.086, 0.25	850—490—230	< 10 ⁴
E	0.26, 0.2	640—410—300	> 10 ⁷
F	0.26, 0.3	930—570—400	< 10 ⁴

^a All nitride samples have doses of 7.2, 9.6, 12 × 10¹⁷ cm⁻² and after 1200–1300 °C for 2 h annealing

^b Corresponding scanning periods for scanning speeds of 0.0086, 0.086 and 0.26 cm s⁻¹ are 1250, 125 and 40 s.

^c Corresponding dose rates for beam currents of 0.15, 0.18, 0.2, 0.25 and 0.3 mA are 7.5, 9, 10, 12.5 and 15 × 10⁻³ mA cm⁻².

Note: $T_{\max}$, T_{av} and $T_{\min}$ denote the maximum, average and minimum wafer temperatures during implant. The defect density was estimated by taking the average number of dislocations (after Wright Etch) inside an area of 0.25 mm² for a number of samples. The dislocations were observed and identified by both OM and SEM. The crystallinity quality has also been checked by XTEM and RBS [3, 4]. The wafer temperature during implant was measured by mounting a thermocouple on a test wafer in a series of test runs at various input power levels and scanning speeds.

Table 2. Buried nitride layer formation.

(A) 0.0086 cm s⁻¹, 1200 °C/2 h.

Dose (× 10 ¹⁷ cm ⁻²)	Beam current (mA)			
	0.05	0.15	0.2	0.4
2.4				—
4.8				a (—)
7.2			a (—)	a-b (b)
9.6			a-b (b)	b (b)
12.0	a (—)	a (—)	a-b (b)	b (b)

(B) 1.2 × 10¹⁸ cm⁻², 1200 °C for 2 h.

Beam current (mA)	Linear wafer scanning speed (cm s ⁻¹)		
	0.0086	0.086	0.26
0.15	a (—)	a (—)	a (—)
0.2	a-b (b)	a (—)	a (—)
0.4	b (b)	b (b)	b (b)

a: Mainly alpha-phase silicon nitride is formed

b: Mainly beta-phase silicon nitride is formed

a-b: Both alpha- and beta-phase silicon nitride is formed

—: Amorphous silicon nitride

Note. Values in parentheses are nitride phases before annealing and the nitride phases were identified by a PW1008 x-ray diffraction set-up.

alpha-nitride is mainly formed during post-implant annealing, beta-nitride is mainly formed by *in situ* recrystallization during the high dose rate and high cycling wafer heating implant (0.2 mA and 0.4 mA). The crystallinity increases with beam current and dose and post-implant annealing leads to further crystallization of the nitride layers in both phases.

In buried nitride soi, alpha-nitride has been well known to be formed. However, very few reports have been found on the existence of beta-nitride. It is known that the conditions for beta-nitride formation from CVD nitride is more stringent than those for the alpha-nitride [6]. Moreover, as shown in table 2, beta-nitride only begins to form at 0.2 mA. Hence we speculate that,

during the special temperature cycling stationary beam implant, there might be some profound dynamic effect which critically favours the nucleation of beta-nitride.

The dependence of the properties of the alpha- and beta-phase nitrides and surface qualities of the crystal Si layers upon the process is shown in table 3. From the results, we found that they are highly comparable to soi substrates prepared using other methods [7, 8]. We also found that the surface Si layer has been highly doped by the nitrogen (n-type) and the active carrier concentration is about $1 \times 10^{18} \text{ cm}^{-3}$. The electron mobility ($110\text{--}140 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) is about half the value for normal Si and the recombination lifetime ($40\text{--}70 \mu\text{s}$) is anomalously high compared with normal Si with similar doping. These effects are probably caused by the high nitrogen content inside the surface Si layer.

Preliminary direct device fabrication of NMOS poly-Si-gate TFTs on this new soi substrate without using epitaxy has also been attempted using the commercial standard $2 \mu\text{m}$ NMOSFET technology. Good transistor action has been observed for the bulk Si control MOSFETs. However, for the SOITFTs, the characteristics of the devices have been found to be distorted and severe retardation of gate oxide growth has been observed.

The oxidation retardation is first reported in buried nitride soi and is believed to be due to the high nitrogen content inside the surface Si layer. By performing a series of oxide growth experiments on all the buried nitride substrates, we found that silicon oxide can only be grown on the surface Si layer after treating at a high tempera-

ture and a long period oxidation of about 1150°C for 9 h. Once oxide is formed, it will then grow at a similar rate as that for unimplanted Si. In the control samples where normal Si wafers have been nitrogen doped to give similar surface peak doping of about $10^{18}\text{--}10^{20} \text{ cm}^{-3}$, only slight oxidation retardation has been observed for various oxidation conditions. The oxide thickness for the control samples is about 20% thinner than that for unimplanted Si and is in good agreement with the nitrogen-implanted Si results [9]. This implies that besides the effect of the high nitrogen content upon the oxide formation on the surface Si layer, other effects might also exist such as the formation of a nitrogen complex or lattice damage.

For buried nitride to be a new contender as an soi substrate, the nitrogen concentration in the surface Si layer needs to be well controlled. Otherwise, many new problems, such as low carrier mobility, high recombination lifetime and oxidation retardation effect, will arise. Novel processes must then be developed for IC devices to be fabricated directly in nitride soi without using epitaxy. As extremely high post-implantation annealing has already been known to give excellent quality buried oxide soi substrates [10], it is of great interest to see how the properties of the buried nitride soi substrates depend on special annealing conditions. Specially designed annealing experiments such as high temperature ($>1300^\circ\text{C}$) and rapid thermal annealing (in vacuum and in other inert gas ambients) are currently under investigation in our laboratory.

Table 3. $7.2\text{--}12 \times 10^{17} \text{ cm}^{-2}$, $1200\text{--}1300^\circ\text{C}$ for 2 h.
(A) Properties of surface silicon layers.

Beam current (mA)	0.05	0.15	0.2	0.4
Crystallinity	poly-Si		←	single-Si →
Dislocations (cm^2)	←	$>1 \times 10^7$	→	← $< \times 10^4$ →
Thickness (nm)			←	about 220 →
Dopant type			←	n-type →
Resistivity			←	about $0.01 \Omega \text{ cm}$ →
Hall mobility ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)			140	110
Minority carrier lifetime ($1 \times 10^{-6} \text{ s}$)			40–50	60–75
(B) Properties of buried nitride layers.				
Beam current (mA)	0.05	0.15	0.2	0.4
Phase		alpha		beta
Refractive index	2.0	2.4	2.6	2.9
Thickness (nm)	350	340	330	300
Leakage current density at $V = 10 \text{ V}$		$50\text{--}5 \times 10^{-6} \text{ A cm}^{-2}$		
Leakage current density at $V = 50 \text{ V}$		about $50 \times 10^{-6} \text{ A cm}^{-2}$		
Resistivity		$2\text{--}20 \times 10^{11} \Omega \text{ cm}$		
Dielectric constant		5.6–6.1		
Charge density		$<5 \times 10^{11} \text{ cm}^{-2}$		
Breakdown voltage		$>100 \text{ V}$		
Breakdown field		$>3 \text{ MV cm}^{-1}$		

4. Conclusion

The feasibility of buried nitride soi substrates prepared using stationary beam synthesis has been studied. Buried nitride soi substrates with surface Si layers of good quality crystal can be formed, provided the *in situ* wafer heating during implantation is sufficiently high. Also, good insulating alpha- and beta-phase silicon nitrides can be formed in the buried nitride layers if the implant and annealing conditions are suitably controlled. Moreover, both the insulating nitride and the residual Si layers have been found to possess good qualities. However, the high nitrogen content inside the residual Si layer has been found to create new problems for direct fabrication of devices on the soi substrate.

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