Frame sequential miniature silicon display using mixed-mode twisted nematic liquid crystal

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ABSTRACT

We present a mixed-mode twisted nematic (MTN) silicon display integrated with 4-bit digital data drivers. With high bandwidth of the digital data driver, pixel access time of less than 10 ns was achieved. Digital gray-scale addressing technique, which utilizes multiple fields per frame, synchronous field voltages and weighted field time, was applied to increase gray scale from 4 to 8 bits. Chromatic characterization of the display using 3-color-in-1 LED as light source was performed. Contrast ratios on pixel array were 49, 32 and 21, respectively, for red, green and blue colors at 3 V root-mean-squared voltage. It was observed that frame inversion gave rise to higher contrast ratio, while column inversion was less color dispersive. Using color sequential technique, we have demonstrated 4 bits per color for this highly integrated MTN display.

Keywords: AMLCD miniature displays, mixed-mode twisted nematic, color sequential

1. INTRODUCTION

Crystalline silicon has been well recognized as an alternative approach for the fabrication of active matrix liquid crystal display (AMLCD)¹. The advantages are better electronic properties and more matured silicon fabrication technology. Very sophisticated driver circuitry and very fine pixel can be integrated together as a self-contained high-resolution display. Monolithic integration of drivers into the display also helps simplify interconnection and packaging problems associated with the display system.

In general, the silicon based AMLCD was integrated with analog data drivers to render gray-scale image². This type of display, usually filled with nematic liquid crystal, can accept directly CRT-compatible analog signal. Another technique relied on integrated binary data drivers and field sequential approach to drive ferroelectric liquid crystal for gray-scale representation³. Digital data drivers of more than 4 bits cannot be effectively integrated into the display due to layout constraint of small pixel pitch. The digital driving scheme has advantages of nature interface to digital systems, high bandwidth and γ -correction for the display.

In our earlier works, we have fabricated a series of AMLCD panels on silicon substrate using CMOS technology with back-end chemical-mechanical polishing for silicon surface planarization^{4,5}. We have also developed a digital gray-scale addressing technique to improve the gray scale limited by the internal digital data drivers⁶. In this work, we present a color sequential technique applied to this highly integrated mixed-mode twisted nematic (MTN) silicon display⁷.

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2. DISPLAY PANEL

Figure 1 shows functional block diagram of the display panel. Only two control signals are required. Whereas, FLM marks the first line, and DISP points the first pixel of each line. The 4-bit pixel data inputs are shifted in series to the data drivers and transferred in parallel to D/A converters where the D/A conversions are performed. The external 4 reference voltages for the D/A converters are for tailoring reflectance-vs-voltage curves of liquid crystal cell with respect to different colors. With integrated high-bandwidth digital data drivers, pixel clock can go up to 100 MHz which corresponds to 10 ns pixel access time. The display panel has 400 by 300 pixels, or 1/4 SVGA resolution. Pixel pitch is 25 μm and fill factor is 91% as a result of 0.8 μm layout rules. Figure 2 shows SEM picture of the pixel array. Surface topographic variation was less than 500 $\text{\AA}$ within pixels.

Figure 1 Functional block diagram of the miniature silicon display panel.

Figure 2 SEM picture of the pixel array.

3. LIQUID CRYSTAL CELL

On top of the silicon panel, we proceeded to make MTN liquid crystal cell. The MTN cell had a 70° twist angle, a 30° polarizer angle and a retardation value of 0.31 μm . The cell gap was 5 μm and ZLI-1965 liquid crystal from E. Merck with a low Δn of 0.0625 was used. Using polarizing beam splitter and ultra bright LED as light source, we have characterized the reflectance-vs-voltage curves for white light and three primary colors on the pixel array. The contrast ratio for white LED illumination was 33:1 at 3 V root-mean-squared voltage (V_{rms}), and was increased to 42:1 at 3.5 V_{rms} . These values was about 55% of the simulated ones which were 60 and 70, respectively⁸. We attributed this discrepancy mainly to the inter-pixel gaps, which affected the liquid crystal alignment. Multi-domain and reversed-twist phenomena were observed on the inter-pixel gaps by microscope. It was also observed that driving techniques affected greatly the reflectance-vs-voltage curves. The contrast ratio measured at column inversion was 65% smaller than that

measured at frame inversion for this 25 μm pixel array. A preliminary optical simulation showed that fringing effect on edges of pixels caused by the column inversion reduced the contrast ratio.

For chromatic characterization, we used 3-color-in-1 LED as light source. With individual control of light emission intensity of each color LED, we were able to tune up an equal-energy white light with color coordinate of $x = 0.33$ and $y = 0.33$. Normalized spectral intensity of the light source is shown in Figure 3. Figure 4 shows the reflectance-vs-voltage curves for three primary colors as characterized by this 3-color-in-1 LED. The contrast ratios were 49, 32 and 21, respectively for red, green and blue light illumination at 3 Vrms. The monotonous decrease in contrast ratio with decreasing wavelength is a characteristic of MTN liquid crystal cell^{7,8}. The contrast ratio was 31 under equal-energy white illumination at 3 Vrms. This value was concurrent with that measured under a single white LED illumination, though a little bit smaller. With polynomial curve fitting of the reflectance-vs-voltage curves as shown in Figure 4, we can proceed to obtain γ -correction resistor network of 16 true gray scales for three primary colors. This γ -correction resistor network was deemed required in order to implement a color sequential display of true color.

Figure 3 Normalized spectral intensity of the 3-color-in-1 LED.

Figure 4 Reflectance-vs-voltage curves for three primary colors.

Figure 5 Traces of equal-energy white light and three primary colors in color space with voltage from 1.0 to 3.0 Vrms.

Figure 5 shows traces of equal-energy white light and three primary colors in color space with voltage from 1.0 to 3.0 Vrms. The white light moved from $x = 0.33$ and $y = 0.33$ of bright state toward $x = 0.22$ and $y = 0.28$ of dark state. Color dispersion was observed as the coordinates changed with voltage, though the change was small. As a result, the display revealed a bluish dark, instead of a true dark. It is interesting to note that driving techniques affect the color dispersion as well. Under column inversion, white light moved toward $x = 0.31$ and $y = 0.29$ of dark state at 3.0 Vrms. Color dispersion was minimal.

4. DIGITAL GRAY-SCALE ADDRESSING TECHNIQUES

The digital gray-scale addressing techniques rely on liquid crystal cell to average dynamic excitation voltages applied to the pixel array for an effective excitation. In standard digital gray-scale addressing technique, there is only one field per frame. The excitation voltage of each pixel is constant for entire frame and gray scale is limited by number of bits of the data driver. With multiple fields per frame, the gray scale can be increased. The total number of gray levels becomes the sum of number of gray levels in each field. However, it is not likely to have more than 4 fields per frame which gives rise to about 4 ms field time that nematic liquid crystal cell cannot fully respond to.

P. M. Alt and his co-workers proposed a digital gray-scale technique in which each field was associated with its own field voltages. He used three fields per frame and binary data driver to achieve 3-bit gray scale or 8 gray levels⁹. This digital gray-scale addressing technique can be applied to the digital-input AMLCD with M -bit digital data drivers as well. Whereas, the field voltages are weighted in 2^{-M} for the consecutive fields. With this approach, the total number of gray levels becomes the product of number of gray levels in each field. However, the 2^{-M} factor of field voltages also attributes to 2^{-M} luminance reduction for the consecutive fields. As a consequence, the luminance is roughly inversely proportional to the number of fields and is greatly reduced. In addition, this generalized digital gray-scale technique requires a least incremental voltage of $(V_{ON} - V_{OFF}) / 2^N$ for N -bit gray scale. For a typical IV linear reflectance-vs-voltage curve, this least incremental voltage is about 4 mV for 8-bit gray scale.

To improve the small luminance and small incremental voltage limitations, we introduced weighted field time. With two fields per frame, the luminance of the generalized digital gray-scale technique is reduced to $(1 + 2^{-M}) / (1 + 1)$ and the least incremental voltage is $(V_{ON} - V_{OFF}) / 2^{2M}$, where M is the number of bits of the data driver and 2^{2M} is the number of gray levels. Let the first field time K times of the second one. The luminance and least incremental voltage become $(K + K \cdot 2^{-M}) / (K + 1)$ and $(V_{ON} - V_{OFF}) / (2^{2M} / K)$, respectively. Both the luminance and the least

incremental voltage are relaxed by about $2K / (K + 1)$ and K times, respectively. The improvement is at the expense of bandwidth which is also increased by $(K + 1) / (1 + 1)$ times. The implementation of this enhanced gray-scale addressing technique is shown in Figure 6.

Figure 6 Schematic of the enhanced gray-scale addressing technique.

Figure 7(a) shows 16 gray scales realized by the inherent 4-bit digital data drivers and Figure 7(b) shows 256 gray scales realized by the enhanced gray-scale technique. Table 1 summarizes system comparison of the standard and enhanced gray-scale addressing techniques applied to the 4-bit MTN silicon display. It is noted that the generalized digital gray-scale technique is a special kind of the enhanced gray-scale technique in which $K = 1$.

Figure 7 (a) 16 gray scales realized by the standard addressing technique and (b) 256 gray scales realized by the enhanced addressing technique.

Table 1 System comparison of standard and enhanced addressing techniques.

Addressing techniques	# of fields per frame	Field time (ms)		Incremental field voltage (mV)		Normalized luminance	Gray levels
Standard	1	16.7		128		100%	16
Enhanced	2	13.4	3.3	128	32	85%	256

5. COLOR SEQUENTIAL TECHNIQUE

Figure 8 shows a schematic of color sequential technique applied to the silicon display. The parallel red (R), green (G) and blue (B) video signals are firstly stored in a buffer memory. Thereafter, R, G and B signals are written into the display in sequence. There are three phases in each R, G or B sub-frame. The first phase is data loading phase in which the corresponding R, G or B sub-frame is loaded. Pixel access time and display resolution determine the period of this phase. With 10 ns pixel access time provided by the high-bandwidth digital data drivers, it takes exactly 1.2 ms to load each sub-frame for the silicon display with 400 x 300 pixels. The second phase is liquid crystal response phase in which liquid crystal responds to loaded sub-frame. The liquid crystal response time, especially the falling time which is usually longer the rising one, determines the minimum length of this phase. The response time of our MTN cell was 18 ms, whereas the rising time was 6 ms and the falling time was 12 ms. A minimum 12 ms liquid crystal response phase is required for the MTN cell to be fully responded. The third phase is LED illumination phase in which corresponding R, G or B LED is turned on and illuminates on the display. LED radiance intensity and system luminance requirement determine the minimum pulse width of this phase. In the experiment, a 2 ms pulse can provide enough luminance for our display with ultra bright 3-color-in-1 LED and a good optical setup.

Figure 8 Schematic of color sequential technique applied to the silicon display.

One of important task in characterization of the color sequential display is to generate an equal-energy white light source for display illumination. In the experiment, we fixed the pulse width of each color LED, but varied its radiance intensity by controlling LED current. The LED pulse width was set to 4 ms at 90 Hz sub-frame rate, and 2 ms at 180 Hz sub-frame rate. Duty cycle was 12% for each color LED in both 90 Hz and 180 Hz sub-frame rates. Figure 9 shows normalized spectral density of equal-energy white light illuminator provided by color sequential 3-color-in-1 LED.

The sub-frame period was 5.6 ms at 180 Hz and was doubled to 11.1 ms at 90 Hz. The data loading phase of each sub-frame was fixed at 1.2 ms using 10 ns pixel access time. As a consequence, time allocation for the liquid crystal response phase was 2.4 ms at 180 Hz sub-frame rate and 5.9 ms at 90 Hz, respectively. Color mixing phenomenon occurred in both cases due to inadequate time allocation for the liquid crystal response phase. Figure 10 shows color coordinates of red, green and blue colors observed directly from LED illumination and observed at 90 and 180 Hz. NTSC standard is also included for comparison. The LED illuminator can provide comparable color purity with NTSC standard as shown in the figure. However, color was mixed through the MTN cell due to slow liquid crystal response. The color sequence was R, G and B as shown in Figure 8. As a result, the red sub-frame was partially illuminated by the green LED because the green LED turned on before the red sub-frame was totally turned off. The red color in color space was therefore shifted toward green as shown in Figure 10. Similarly, green color was shifted toward blue, and blue color was shifted toward red. Color mixing phenomenon was more evident at 180 Hz as compared with that at 90 Hz.

Figure 9 Normalized spectral intensity of the equal-energy white light illuminator.

Figure 10 Color coordinates of red, green and blue colors observed from LED illumination, and observed at 90 and 180 Hz. NTSC standard is included for comparison.

Figure 11 shows traces of each primary color and white light at different gray scales from bright to dark states. Color purity was reduced as the display turned dark. The liquid crystal cell could not fully respond with voltage due to inadequate time allocation for the liquid crystal response phase. As a result, the display could not reach its best dark or bright state before the next sub-frame starts. Contrast ratio of each primary color under color sequential equal-energy white light illumination was therefore reduced. It was observed that the contrast ratios of three primary colors were reduced by about 60% at 180 Hz, and by about 20% at 90 Hz. The contrast ratios of primary colors, especially the blue one, were still larger than 16 at 90 Hz. As a consequence, we could obtain 16 gray scales for all primary colors and hence, 4096 true colors for the display.

Figure 11 Color spectrum for the color-sequential MTN display at 90 Hz.

With chromatic characterization data as guideline, we proceeded to design a miniature silicon display interfaced with personal computer (PC). We retrieved every other frame of the 60 Hz video signals from the PC and write in sequence into the display at 90 Hz sub-frame rate. Frame inversion was used for high contrast ratio and γ -correction resistor network was included for true gray-scale representation. Figure 12 shows color viewgraphs of the silicon display interfaced with PC. Vivid images of 4096 colors were demonstrated.

Figure 12 Color viewgraphs of the miniature silicon display.

6. CONCLUSION

In summary, we have presented a highly integrated color sequential silicon display using mixed-mode twisted nematic liquid crystal. Digital gray-scale address technique which utilizes multiple fields per frame, synchronous field voltages and weighted field time, was applied to increase gray scale from 4 to 8 bits. Chromatic characterization of the display using 3-color-in-1 LED as light source was performed. Contrast ratios on the pixel array were 49, 32 and 21, respectively, for red, green and blue colors at 3 Vrms. It was observed that frame inversion gave rise to higher contrast ratio, while column inversion was less color dispersive. With high bandwidth of digital data driver, pixel access time of

less than 10 ns was achieved. Using color sequential technique, we have demonstrated 4 bits per color for this highly integrated MTN display at 90 Hz sub-frame rate.

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8. REFERENCE

1. See for example, P. M. Alt, "Single Crystal Silicon for High Resolution Displays" Conf. Record, 1997 Int. Display Research Conf. pp.19-28, 1997.
2. J.P. Salerno, "Single Crystal Silicon AMLCDs". Conf. Record, 1994 Int. Display Research Conf., pp. 39-44, 1994.
3. D.H. Banas, J. Cunningham, M. Handschy, M. Meadows and D. Ward, "Ferroelectric Liquid-Crystal Spatial Light Modulators for Projection Display", Proc. of SPIE, Vol. 2650, pp. 229-232, 1996.
4. H.C. Huang, P.W. Cheng, W.C. YIP and H.S. Kwok, "AMLCD on a Silicon Substrate with Integrated Digital Data Driver", Proc. of the 15th Int. Display Research Conf., pp. 481-484, 1995.
5. H.C. Huang, Y.T. Wong, C.T. Nguyen and H.S. Kwok, "Planarization of Liquid-Crystal-on-Silicon Projection Display with Multilevel Metallization and Chemical-Mechanical Polishing", 1996 SID Int. Symposium, Digest of Technical Papers, pp. 685-688, 1996.
6. H.C. Huang, P.W. Cheng and H.S. Kwok, "An Enhanced Gray-Scale Addressing Technique for Digital-Input AMLCD on Planarized Silicon Substrate", 1996 SID Int. Symposium, Digest of Technical Papers, pp. 489-492, 1997.
7. S.T. Wu and C.S. Wu, "Mixed-mode twisted nematic liquid crystal cells for reflective displays", Appl. Phys. Lett., Vol.68, No.11, pp.1455-1457, 1996.
8. J. Chen, F.H. Yu, S.T. Tang, H.C. Huang and H.S. Kwok, "New Optimized Reflective LCD Modes for Direct-View and Projection Displays", 1997 SID Int. Symposium, Digest of Technical Papers, pp. 639-642, 1997.
9. P.M. Alt, C.G. Powell, B.L. Owens Jr., H. Ifill, "A gray-scale addressing technique for thin-film-transistor/liquid crystal displays", IBM J. Res. Develop. Vol. 36 No. 1, pp. 11-22, 1992.