Noise Coupling in Heavily and Lightly Doped Substrate from Planar Spiral Inductor

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Abstract— Recently, much studies have been done to include on-chip inductors for wireless communication IC design. The large area metal plane of the spiral inductor can form large capacitor to the silicon substrate. At high enough frequency, excitation of the inductor will induce noise to the substrate. In this paper, we will present the simulation results of the coupling effect of a planar spiral inductor on heavily and lightly doped substrate by using a compact model of the substrate. Results show that the insertion of a P+ diffusion guard ring can reduce about 15dB of noise for lightly doped substrate and 7dB of noise for heavily doped substrate at 3GHz. Variation in the size of the P+ diffusion guard ring affects the efficiency of noise reduction and also the inductance. Results show that in order to optimize for inductance, the side length of the guard ring needs to be twice the side length of the inductor and the guard ring can only reduce about 6dB of noise for lightly doped substrate and 1.5dB of noise for heavily doped substrate at 3GHz.

I. INTRODUCTION

IN the past few years, experimental studies and modeling techniques have been done on substrate noise coupling in analog/digital mixed signal system for both lightly and heavily doped substrate[1][2][3]. We studied here another source of substrate noise that occurs at high frequency. In high frequency, we often use on-chip inductors for reactive loading and matching purposes. The large area metal plane of the spiral inductor can form large capacitor to the silicon substrate and at high enough frequency, excitation of the inductor will induce noise to the substrate. In common practice, inductors can be fabricated by using top-layer metals, and the size of an inductor can span as large as $500 \times 500 \mu\text{m}^2$. The inductor forms large coupling capacitance between silicon oxide and propagates the noise to the substrate at high frequencies. Several techniques have been suggested[2] to reduce the substrate noise, and in this paper, we will attempt to minimize the coupling noise from the planar spiral inductor to other area on the chip by using P+ diffusion guard ring. Inductor guard ring will increase the efficiency of noise reduction, but at the same time it reduces the inductance of the spiral inductor. We studied the optimum size of the guard ring for efficient noise reduction and the largest possible inductance of the spiral inductor for both lightly and heavily doped substrate.

In order to have a rapid and accurate prediction of the substrate noise coupling for lightly and heavily doped substrate, a compact model is needed for simulation. Device simulators such as PISCES can be used to obtain a detailed

understanding of the crosstalk mechanisms, but cannot be efficiently used at the circuit level because they require a large amount of computing power, which limits the application of such tools to a few devices. The AWE approach provides a rapid tool for predicting the substrate coupling effect, and in this paper we will use LAYIN[4] to extract a simple compact model of the substrate for simulations.

Fig. 1. Layout of the simulation used in LAYIN

II. SIMULATIONS

LAYIN requires a physical layout and a specific technology description to generate a simple macromodel for the heavily and lightly doped substrate, and the model is represented in a SPICE subcircuit netlist. The layout representation includes the perturbing (inductor) and sensitive (P+ contact) sections, as well as substrate connections to ground (guard ring). Fig. 1 shows the layout used in the model extraction by LAYIN. MOSIS $2\mu\text{m}$ CMOS Nwell process doping profiles are used as the technology description for the lightly doped substrate and the MOSIS $0.8\mu\text{m}$ CMOS Nwell process doping profiles are used for the case of heavily doped substrate. Fig. 2 shows the resistivity plot for spreading resistance analysis of a device wafer fabricated with the MOSIS $0.8\mu\text{m}$ process. From the resistivity plot, we can generate the technology description for that particular process, which will be used by LAYIN during model extraction. Fig. 3 shows the LAYIN process flow.

Fig. 2. Measured substrate resistivity plot of the $0.8\mu\text{m}$ MOSIS process by spreading resistance analysis (SRA)

Fig. 3. LAYIN process flow

A. Effect of physical separation between inductor and P+ diffusion contact

A 2nH inductor of size $350\mu\text{m} \times 350\mu\text{m}$ is used as a perturbing source with $7\mu\text{m}$ edge to edge distance between conductors and $40\mu\text{m}$ conductor width. A $50\mu\text{m} \times 50\mu\text{m}$ P+ diffusion contact is located at various distance d from the centre of the inductor which serves as a noise sensor. A P+ diffusion guard ring with $25\mu\text{m}$ conductor width surrounding the inductor is used to observe the reduction of substrate noise when the guard ring is grounded.

By stimulating the inductor and tracking the noise signal pick up at the P+ diffusion contact at various physical separation from the inductor, the relative reduction in the noise level for various distances can be observed for cases when guard ring is present or absent. In this study, we will compare the reduction in noise level by using the scattering parameter S_{21} . The two port network comprised of the inductor as the input and the P+ diffusion contact as the output and the lower the magnitude of S_{21} the better is the isolation of noise. Fig. 4 & 5 shows the cross section of the layout for heavily and lightly doped substrate respectively.

In the simulations, the P+ diffusion guard ring which is around the inductor will be removed for cases in order to compare the gain in the reduction of noise.

Fig. 4. Cross section of the layout for heavily doped substrate

Fig. 5. Cross section of the layout for lightly doped substrate

Fig. 6 shows the isolation characteristics (S_{21}) from the inductor to P+ diffusion contact in lightly doped substrate. From the data shown in Fig. 6, it is clear that with the insertion of guard ring, it helps to reduce the noise level at various distance d from the centre of the inductor, but the reduction of noise level is gradually decreasing at high frequency. At 3GHz , the S_{21} is reduced about 20dB for small distance d and about 15dB for large distance d when the guard ring is inserted. Fig 7 shows the details of the reduction of noise for various distance d between the inductor and the P+ diffusion contact, when the distance increase from $200\mu\text{m}$ to $800\mu\text{m}$, S_{21} is reduced by 17dB when the guard ring is not inserted and reduced by 12dB when guard ring is inserted.

For the case of heavily doped substrate, the situation is quite different from that in the lightly doped substrate e.g. the reduction of noise level is less than that in the lightly doped substrate when the guard ring is inserted. Fig. 8 shows the isolation characteristics (S_{21}) from the inductor to P+ diffusion contact in heavily substrate. From the data shown in Fig. 8, the S_{21} is reduced by about 7dB when the guard ring is inserted and the effect of physical separation between the inductor and P+ diffusion contact is very small. Fig. 9 illustrate the noise reduction is small (less than 2dB) for large variation of distance d from $200\mu\text{m}$ to $800\mu\text{m}$.

B. Effect of variation in the size of the guard ring

Besides the effect of the physical separation between inductor and substrate contact, the size of the guard ring can also affect the level of noise reduction and also the inductance. Ideally, for noise reason, one would want the guard

Fig. 6. Simulated S_{21} characteristics from inductor to substrate contact vs frequency for lightly doped substrate. At high frequency, substrate noise is seen and efficiency of the guard ring diminishes.

Fig. 7. S_{21} characteristics at 3GHz vs substrate contact distance d for lightly doped substrate. With the insertion of guard ring, S_{21} can reduce by 15dB, but when we want to optimize for inductance and increase r from $175\mu m$ to $325\mu m$, only 6dB of noise can be reduced.

ring to be close to the inductor. If the guard ring is smaller than the inductor coil, portion of the inductor outside the ring cannot be shielded.

Fig. 10 shows how the S_{21} parameter changes as the guard ring distance r varies. The S_{21} parameter is measured from the inductor to a substrate contact with $d=375\mu m$. As shown in Fig. 10, the trend of variation in S_{21} parameters are similar for the two kind of substrate, and the optimal guard ring distance r for the maximum noise reduction occurs when r is around $175\mu m$ (edge of inductor) for lightly doped substrate and around $140\mu m$ for heavily doped substrate. In other words, maximum noise reduction can be achieved when the size of the guard ring is about the same as the size of the planar inductor. A practical case will be when the guard ring is just next to the edge of the inductor to provide maximum noise reduction for the lightly doped substrate.

Fig. 8. Simulated S_{21} characteristics from inductor to substrate contact vs frequency for heavily doped substrate. Physical separation does not help much in reducing noise.

Fig. 9. S_{21} characteristics at 3GHz vs substrate contact distance d for heavily doped substrate. With the insertion of guard ring, S_{21} can reduce by 7dB, but when we want to optimize for inductance and increase r from $175\mu m$ to $325\mu m$, only 1.5dB of noise can be reduced.

Unfortunately, while maximum noise reduction can be achieved when the guard ring is about same size as the inductor, inductance will also be affected when size of guard ring is close to that of the inductor due to mirror effect. In order to find out how the inductance be affected when the guard ring is inserted, we use Maxwell Quick 3D Parameter Extractor[5] to simulate cases for different size of guard rings. Fig. 11 shows the variation of inductance with the guard ring distance r . When the guard ring distance r reaches $140\mu m$, the inductance will drop to less than $1nH$, which is less than half of the original value and when r reaches $175\mu m$, the inductance is about $1.55nH$.

As illustrated above, when we need to have maximum noise reduction for lightly and heavily doped substrate the inductance will drop to $0.98nH$ and $1.55nH$ respectively, so there is a tradeoff between noise reduction and inductance and we need to sacrifice one to gain another.

On the other hand, if we want to optimize for inductance, the guard ring distance r need to be greater than $325\mu\text{m}$ in order to achieve inductance of 1.96nH (See Fig. 11). As illustrated in Fig. 7 and Fig. 9 when the guard ring distance r is increased from $175\mu\text{m}$ to $325\mu\text{m}$, the improvement of noise reduction with the insertion of guard ring will be reduced from 15dB to 6dB for lightly doped substrate and from 7dB to 1.5dB for heavily doped substrate. So in order to optimize for inductance, the side length of the guard ring need to be about twice the side length of the spiral inductor, and the efficiency of the guard ring in reducing noise at substrate contacts will be decreased by 9dB and 5.5dB for heavily and lightly doped substrate respectively.

Fig. 10. S_{21} characteristics at 3GHz vs Guard Ring Distance r when the substrate contact distance $d=375\mu\text{m}$. Maximum noise reduction for heavily and lightly doped substrate occurs when $r=140\mu\text{m}$ and $r=175\mu\text{m}$ respectively.

Fig. 11. Inductance vs Guard Ring Distance r . When maximum noise reduction for heavily and lightly doped substrate occurs, the inductance is 1.55nH and 0.98nH respectively. When optimize for inductance, the side length of the guard ring need to be twice the side length of the inductor.

III. CONCLUSION

It has been shown that the P+ diffusion guard ring provides better noise reduction in lightly doped substrate than in heavily doped substrate, and the physical separation

between inductor and substrate contact is another useful mean of reducing substrate noise for lightly doped substrate. While both approaches can reduce the noise level at low frequencies, their benefits are reduced at high operating frequencies. Guard ring seems to be more effective in reducing noise when compared to physical separation for heavily doped substrate. Inductance will be reduced in the presence of the guard ring, and as a tradeoff, maximum noise reduction can be achieved at the expense of reduction in inductance. The simulation results presented in this paper provide an understanding of the effects causing substrate noise from planar spiral inductor through the heavily and lightly doped substrate.

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