A Three-Terminal SOI Gated Varactor for RF Applications

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Abstract --- This paper presents a new CMOS compatible SOI gated varactor for use in RF ICs. With its additional third terminal, the device offers an exceptional large tuning range and a good quality factor. The result of the MEDICI simulation of the structure of the varactor has been confirmed with measured data. A VCO circuit that can potentially exploits the three-terminal property is also reported.

Index: RF, varactor, SOI, passive components

I. INTRODUCTION

In this paper, we present a three terminal gated structure for use as varactors in SOI technologies. The superior speed advantage of the SOI devices has attracted attention in their deployment in both digital and radio frequency (RF) applications [1][2]. Varactor is a critical ingredient in the design of RF voltage controlled oscillator. However, because of the thin film nature of SOI devices, traditional reverse-biased PN diode used in bulk design is not area-efficient [3][4]. Recently, there have been a number of discussions in using accumulation mode MOS capacitor as varactors in bulk technologies [6][6]. The technique should be quite feasible in thin film SOI technologies as well. The accumulation mode varactor can theoretically achieve quite a high quality factor. Yet, the maximum capacitance variation of the accumulation mode varactor is limited to the difference between C_{ox} and the minimum depletion capacitance. And, the sensitivity is limited by the classic CV characteristics of the MOS device. In the gated varactor presented here, a third terminal and an opposite source/drain doping are incorporated to add another degree of freedom to the capacitance-bias relationship. The end result is a varactor that has high quality factor, large tuning range, and high sensitivity. The varactor is implemented in a CMOS compatible SOI process. It achieves a quality factor of more than 150, a large tuning range of $\pm 74\%$ (11.76 pF $\sim$ 1.73 pF) and a sensitivity greater than 7.5 pF/V at 1 GHz.

In Section II, we explain the mechanism of operations. In Section III, we report the measurement and simulation data. Effect of channel length is also discussed. In Section IV, we describe a VCO circuit that can potentially exploit the unique three-terminal property of the gated varactor.

II. MECHANISM OF OPERATION

The SOI gated varactor consists of a lateral N+/N-/P+ diode and an additional gate node fabricated on SOI material. The structure is compatible with ordinary CMOS IC process and is similar to that of PMOSFET. The only exception is that the P+ drain is replaced with an N+ type drain. The structure of the device is shown in Fig. 1. In our ensuing discussions, unless otherwise stated, we assume that the P+ source node is tied to ground. Capacitance changes are observed when a varying voltage is applied either on the gate as V_g or on the drain as V_d .

The circuit model of the gated varactor is shown in Fig. 2(a). C_{pn} refers to the PN junction capacitance between the P+ node and the N- region under the gate oxide. C_g is the gate capacitance between the gate and N- region, R_s' is the resistance between N- region and N+ node, R_d is the source and drain resistance, and R_g is the gate resistance. The equivalent series capacitance C_s at the N+ node includes C_{pn} and C_g . An increase in V_d expands the depletion region and decreases C_s .

When the applied voltage V_g is far above the flatband voltage V_{FB} , the silicon surface of the N- region under the gate is accumulated with electrons provided by the N+ region and the capacitance C_g is at a maximum (simply the oxide capacitance C_{ox}) at $V_d = 0$ V. As V_d increases, the silicon surface varies from accumulation to depletion. The N- region under the gate is depleted and the capacitance C_s decreases. When the N- region of PN junction under the gate is fully depleted, C_s hardly varies with the bias voltage and reaches a minimum. The minimum

capacitance depends mainly on the thickness of the SOI film. Thus, both the gate node and the drain node can be used to alter the equivalent capacitance C_s .

MEDICI simulation was used to verify the above assertion. The result is shown in Fig. 3. The SOI film thickness is 0.1 μm . The buried oxide is 0.37 μm thick. Oxide thickness is 105 Å. The N-region is uniformly doped at $2 \times 10^{17} \text{cm}^{-3}$. The gate length is 0.9 μm . The device is simulated with AC analysis at 1 GHz. The structure is assumed to be 3000 μm wide. When V_d is 0V and V_g is 1.5 V, C_s is largest. As a matter of fact, at that point, C_s is just equal to C_{ox} . The capacitance variation is slightly faster than that of an accumulation-mode varactor [6]. When V_d changes, both C_{pn} and C_g change. The improvement in sensitivity, however, varies depending on the ratio of C_{pn} and C_g , and should roughly be linearly proportional to t_{si}/L of the device. Being a three-terminal varactor, the capacitance variation produces a family of curves. These properties potentially offer a larger capacitance variations if both V_g and V_d are allowed to change.

Fig. 4a gives the MEDICI simulation results of the capacitance-voltage relationships and the quality factor Q with different lengths L . At long L , the C_s is larger due to a larger gate oxide capacitance. Since the point at which the silicon film is completely depleted is independent of length, the rolloff at long L is more rapid. Fig. 4b shows the Q factor as a function of L at $V_g=0$ V. Q is equal to $1/\omega R_s C_s$. The larger C_s at long L diminishes the Q since it is not accompanied by an equal reduction of R_s . The sudden jump of Q from the low V_d region to the high V_d region can be appreciated with the aid of Fig. 2. The dashed line in the N-body indicates the extension of the depletion region as V_d increases. When V_d increases, the non-depleted region is compressed

downward and at the same time pushed towards the N+ region. While the compressed downward phenomenon increases R_s , the push towards the N+ region reduces R_s . For small V_d , an increase in V_d induces a net increase in R_s . R_s drops beyond a certain V_d depending on the channel length.

III. RESULTS AND DISCUSSIONS

The experimental gated varactors were fabricated on a SOI CMOS process. The thickness of the SOI film is 0.1 μm . The gate oxide is 105 Å, and the buried oxide thickness is 0.37 μm . The channel length is 0.9 μm , respectively. The effective width is 3000 μm . The width of the drain and the source is 1.2 μm . The doping concentration of N- region is $2 \times 10^{17} \text{ cm}^{-3}$. To achieve maximum area efficiency, a multi-finger gate is adopted. The structure fits in a compact area of less than 20 μm by 300 μm .

S-parameter measurements were carried out using an HP8510C Network Analyzer and Cascade Microtech coplanar ground-signal-ground probes. The equivalent series capacitance C_s are extracted under $L = 0.9 \mu\text{m}$ different gate voltages V_g and plotted in and Fig. 5. The quality factor Q is given in Fig. 6. The measured C_s is larger than that simulated. The difference emanates from the multi-finger structure which contributes inter-finger capacitance. The extra capacitance was not accounted for in our two-dimensional simulation. At $V_g=1.5\text{V}$, varying V_d allows for a tuning range of $\pm 74\%$ and the sensitivity is 2.5 pF/V. The quality factor is above 15. For $V_g=-1.5 \text{ V}$, the tuning sensitivity is $\pm 39\%$ The maximum Q is 110. The tuning sensitivity is defined as

$$\pm \frac{C_{max} - C_{min}}{C_{max} + C_{min}}$$

Here we define the maximum Q as the largest quality factor that the varactor can achieve before the body is completely depleted.

IV. Possible Circuit Implication

One of the salient features of gated varactor is that it has one additional terminal as compared to either the reverse-biased PN junction varactor or the accumulation-mode varactor. In Fig. 7, we replot the varactor characteristics, but this time we are sweeping V_g . When V_d is fixed, the device functions like the accumulation mode varactor, and the theoretical maximum capacitance change is C_{ox} . The actual capacitance changing range is smaller since at the lower limit, there will be finite parasitic plus depletion capacitance. As seen in Fig. 7, we will be able to enhance the sensitivity if we can vary V_d as well. In Fig. 7, for instance, sensitivity is increased if capacitance can change from Pt. A ($V_d=0V$, $V_g=1.5V$) to Pt. B ($V_d=1V$, $V_g=0.5V$).

In Fig. 8, we illustrate a potential circuit topology. The circuit consists of a cross-coupled pair M_6 and M_7 which, together with the LC tank, forms the core of the oscillator. C_1 and C_2 are two gated varactors whose capacitance varies depending on the biasing at V_g and V_{tune} . In this circuit, the V_d that we have defined in the above section is now equal to difference between the output voltage (V_{out}^+ or V_{out}^-) and a level shifted V_{tune} . As an example to illustrate the possibility of traversing from Pt. A to Pt. B in Fig. 7, assume that we can bias the circuit such that V_{out}^+ and V_{out}^- are at 2 V. In addition, the gate-source difference of M_4 is at 0.5V. With that assumption, V_d tracks linearly with V_{tune} with a 1.5 V difference ($V_d = 1.5 V - V_{tune}$). If we further allow V_{tune} to directly

connect with V_g , then when V_{tune} is 1.5 V, V_g is 1.5 V and V_d is 0 V (*Pt. A*). And, when V_{tune} is 0.5V, V_g is 0.5V and V_d is 1V (*Pt.B*). The achieved capacitance sensitivity of 7.5 pF/V is 178% to 227% larger than that can be achieved with either V_d fixed or V_g fixed in the same region. With V_d fixed at 0V, the capacitance sensitivity is 4.2 pF/V when V_g changes from 0V to 1.5 V, while that with V_d fixed at 1.5 V, the capacitance sensitivity is 3.3 pF/V. Similarly, when V_g is fixed at 0.5 V and 1.5 V, the capacitance sensitivity is 3.3 pF/V and 4.2 pF/V respectively when V_d changes from 0 V to 1.5 V. At this point, it is worthy to mention that the frequency of operation will depend on the values of the L and C in the tank circuit, and that the value of the C is scalable with the width of the varactor.

V. CONCLUSIONS

We demonstrate here a three-terminal gated varactor that achieve a high quality factor and at the same time offers a high tuning range. The gated varactor is completely compatible with CMOS technologies.

VI. ACKNOWLEDGMENT

The authors are thankful to Motorola Semiconductors and HKUST MFF for their support.

VII. REFERENCES

- [1] Markus Zannoth, Bernd Kolb, Josef Fenk, Robert Weigel, "A fully integrated VCO at 2 GHz", *1998 IEEE Solid-State Circuit Conference, Digest of Technical Papers*, pp. 224-225, Feb, 1998.
- [2] Digh Hisamoto, Satoshi Tanaka, Takuma Tanimoto, Shin'ichiro Kimura, "Suspended SOI structure for advanced 0.1 μm CMOS RF devices", *IEEE Transactions on Electron Devices*, vol. 45, no. 5, May 1998, pp. 1039-1046.
- [3] S. M. Sze, *Physics of Semiconductor Devices, 2nd Edition*, Wiley, pp. 114-116.
- [4] J. N. Burghartz, M. Soyuer, K. A. Jenkins, "Integrated RF and microwave components in BiCMOS technology", *IEEE Transactions on Electron Devices*, vol. 43, pp. 1559-1570, Sept. 1996.

- [5] T. Sorraphanth, C. P. Yue, D. K. Shaeffer, T. H. Lee, S. S. Wong, "Analysis and optimization of accumulation -mode varactor for RF ICs", *Digest of Technical Papers, Symposium on VLSI Circuits*, 1998, pp.32-33.
- [6] R. Castello, P. Erratico, S. Manzini, F. Svelto, "A +/- 30% tuning range varactor compatible with future scaled technology", *Digest of Technical Papers, Symposium on VLSI Circuits*, 1998, pp.34-35.

List of Figures

Fig. 1 Structure of the SOI gated varactor. t_{ox} is 105 Å. t_{si} =0.1 μ m, N-body is doped to $2 \times 10^{17} \text{ cm}^{-3}$. Channel length is 0.9 μ m. The simulated device is 3000 μ m wide.

Fig. 2(a) Equivalent RC model of the gated varactor. (b) Depletion of N- region extends as V_d increases.

Fig. 3 Simulation results of the C_s - V_d . The maximum capacitance is C_{ox} , while the minimum is the parasitic capacitance.

Fig. 4 Simulation results of the (a) C_s - V_d and (b) Q - V_d relationships with different lengths L .

Fig. 5 Measured C_s vs. V_d .

Fig. 6 Measured Q .

Fig. 7 Replot of the measured data with the x-axis changed from V_d to V_g .

Fig. 8 A proposed VCO circuit implementation. The circuit can achieve 7.5 pF/V if V_g and V_{tune} are connected to form just one controlling node.

Figure 1

(a)

depletion region extends as reverse bias increases (N-body)

(b)

Figure 2

Figure 3

Figure 4

Figure 5

Figure 6

Figure 7

Figure 8