A Reliability Comparison of Electroplated and Stencil Printed Flip-Chip Solder Bumps Based on UBM Related Intermetallic Compound Growth Properties

Jing-Feng Gong, Philip C. H. Chan, *Senior Member, IEEE*, Guo-Wei Xiao, Ricky S. W. Lee, *Senior Member, IEEE*, and Matthew M. F. Yuen, *Senior Member, IEEE*

Abstract—The effects of under bump metallurgy (UBM) microstructures on the intermetallic compound (IMC) growth of electroplated and stencil printed eutectic Sn-Pb solder bumps were investigated. The process parameters and their effects on UBM surface morphology and UBM shear strength were studied. For the electroplating process, the plating current density was the dominant factor to control the Cu UBM microstructure. For the stencil printing process, the zincation process has the most significant effect on the Ni UBM surface roughness and Ni grain sizes. In both processes, the good adhesion of UBM to aluminum can be obtained under suitable UBM processing conditions. Samples with different UBM microstructures were prepared using the two processes. The resulting samples were thermal aged at 85 °C, 120 °C, and 150 °C. It was observed that the Cu UBM surface roughness had larger effect on the IMC growth and solder ball shear strength than the Ni UBM surface roughness. The thickness of Cu_3Sn and Cu_6Sn_5 IMC depended strongly on the UBM microstructure. However, for Ni/Au UBM, no significant dependence was observed. More likely, the thickness of Au-Ni-Sn IMC near the IMC/solder interface was controlled by the amount of gold and the gold diffusion rate in the solder. Shear tests were performed after thermal aging tests and thermal/humidity tests. Different failure modes of different sample groups were analyzed. Electroless Ni UBM has been developed because it is a mask-less, low-cost process compared to electroplated Cu UBM. This study demonstrated that the process control was much easier for Ni UBM due to its lower reactivity with Sn material. These properties made Ni UBM a promising candidate for the lead-free solder applications.

Index Terms—Copper, electroless Ni, electroplating, flip-chip, intermetallic compound (IMC), reliability, stencil printing, zincation.

I. INTRODUCTION

THE DEMAND for high input/output (I/O) density, cost effective, reliable packaging has increased with the continuing growth of semiconductor industry. The solder-bumped flip-chip technology has many advantages over the traditional

packaging including high density, high I/Os, high electrical performance, low packaging profile [1]. Many different solder bumping processes have been developed. Among them electroplating process is one of the most well established bumping methods. The process includes metal deposition; thick photore-sist patterning; copper stud and eutectic solder electroplating and reflow. Recently, stencil printing has become more popular because it eliminates expensive vacuum sputtering and photolithography process and thus offers a more cost effective bumping method. The process involves pad pretreatment/activation, electroless Ni plating, solder paste stencil printing and reflow.

The reliability of solder bumps is always the primary concern of any bumping process. The excessive intermetallic compound (IMC) formation is always the source of the solder bump failures because of its brittleness property. The effect of IMC on the solder ball reliability has been studied by many researchers [2], [3]. However, the under bump metallurgy (UBM) microstructure, particularly the effect of UBM surface roughness on the IMC growth has not been fully investigated. Furthermore, the comparison of IMC growth and the reliability of Cu-based solder bump and Ni-based solder bump with a different UBM microstructure has not been addressed.

The Cu UBM is formed by electroplating. The microstructure of Cu UBM is determined by many factors including bath temperature, electrolyte composition, and additive amount etc. One of the most critical factors is the plating current density. Large current density causes coarse Cu grain and rough UBM microstructure. However, small plating current density lengthens the plating process and decreases the production throughput. The understanding of the relationship between plating current density and solder bump reliability is critical to the optimization of reliability, yield and production throughput.

The Ni/Au has been widely used as a surface finish in electronic packaging industry for many years. The surface morphology of Ni bumps is controlled by solution type (acid or alkaline), agitation, bath temperature, stabilizer concentration and particularly, the pretreatment or the zincation of aluminum pads. The double zincation process has been used as an industry standard because it provides finer and more uniform zinc coating and therefore smoother Ni UBM surface than the single zincation [4]. However, whether this surface roughness difference has adverse effect on the reliability of flip-chip solder bump has not been investigated in detail and is one of the objectives of this research. The immersed Au acts as oxidation barrier and wetting

Manuscript received July 30, 2003; revised October 11, 2004. This work was supported by the Microelectronics Fabrication Facility (MFF) and Electronic Packaging Center (EPACK), HKUST 6108/03E, Shipley Asia, Ltd., and ITS/196/00. This work was recommended for publication by Editor-in-Chief A. Bar-Cohen upon evaluation of the reviewers' comments.

J.-F. Gong, P. C. H. Chan, and G.-W. Xiao are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: cegjf@ust.hk).

R. S. W. Lee and M. M. F. Yuen are with the Department of Mechanical Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: meymf@ust.hk).

Digital Object Identifier 10.1109/TCAPT.2006.

Fig. 1. Process flow of electroplating process.

Fig. 2. Process flow of stencil printing process.

layer. The deleterious effect of Au was reported to be caused by its reaction with Sn and Ni at the UBM and the solder interfaces in BGA packaging [5]–[7]. In this study, the effect of UBM surface roughness on the Au reaction in flip-chip solder bump will be examined. Two reliability tests were performed for the samples based on the two bumping processes. The tests were: 1) high temperature storage test at 85 °C, 120 °C, and 150 °C and 2) temperature and humidity test under HAST condition. The shear strengths of solder bumps were evaluated by shear test at different stages and are correlated to the IMC growth and microstructure of UBM.

II. EXPERIMENTAL PROCEDURE

A. Sample Preparation

Electroplating: 4-in wafers were sputtered with aluminum and were patterned to form daisy chain test structures. The silicon dioxide passivation was deposited. 80 μm diameter openings were patterned on the aluminum pads. 1000 Å Ti/W and 4000 Å Cu adhesive and barrier layers were sputtered. A positive photoresist with 100 μm opening was used as the mask for the Cu stud and eutectic Sn–Pb solder bump electroplating. After the plating, the photoresist and the exposed adhesive/barrier layer films were removed. The reflow process was conducted under a typical reflow profile with a peak temperature of

220 °C. The solder ball height was $100 \mu\text{m} \pm 4 \mu\text{m}$. Cu UBM with four surface roughness values were prepared by varying the plating current density from 10 mA/cm^2 to 60 mA/cm^2 at 25 °C during copper electroplating. The fabrication process flow is summarized in Fig. 1.

Stencil Printing: Aluminum (AlSi1%) film of 1 to 1.5 μm thickness was sputtered on the 4-in wafers and was patterned by the standard photolithography process described in the previous paragraph. The zincation pretreatment was performed to remove native oxide and activate Al surface. The nickel bumps were selectively plated on the activated aluminum pads by immersing the wafer in the electroless nickel plating solution. A thin layer of Au was deposited on top of the nickel bumps by Au immersion for oxidation protection and solderability. A DEK260 stencil printer was used to print fine-meshed type 5 solder paste (particle size: 15 μm to 25 μm) on the wafers. The reflow process was conducted with the typical eutectic solder reflow profile characterized by a peak temperature of 220 °C. The solder ball height was $100 \mu\text{m} \pm 5 \mu\text{m}$. Two sample groups were prepared. One group of samples labeled as “S” were processed by the single zincation process and the other group labeled as “D” were processed by the double zincation process. Ni bumps with different surface roughness were produced based on two zincation processes. The fabrication process flow is summarized in Fig. 2.

TABLE I
CU UBM SURFACE ROUGHNESS

	Current density (mA/cm ²)	Ra (Å)
SR-1	17	1885
SR-2	36	2459
SR-3	41	4516
SR-4	60	8914

B. Reliability Tests and Sample Inspection

The Cu and Ni UBM surface roughness was measured using a surface profilometer. The solder bumps on different UBMs were placed in a Vulcan 3–550 furnace for thermal aging at 85 °C, 120 °C, and 150 °C for 50, 200, 400, 600, 800, 1000 h. The temperature and time deviation were maintained within 1 °C and ± 5 min. The temperature-humidity test was performed under the condition of 120 °C, 85% RH for 120 h. The solder bump shear strength was measured using a Dage 4000 multipurpose tester at various thermal aging time points. The samples at all thermal aging conditions were cross-sectioned using epoxy molding, grinding and polishing to characterize the interfacial and the internal microstructure of the solder bumps. IMC growth and composition were observed using various techniques including optical microscopy, scanning electron microscopy (JEOL 6300 SEM) and energy dispersive X-ray (Oxford INCA EDX).

III. RESULTS AND DISCUSSION

A. UBM Process and UBM Microstructure

Electroplating: During the copper electroplating, four sample groups with various Cu surface roughnesses were prepared by varying Cu plating current densities. The process parameters for the eutectic solder electroplating were kept the same for all sample groups. Four Cu surface roughness data labeled as SR-1 to SR-4 are distinguished by their arithmetic average (RA) values as shown in Table I. For each group, 25 locations distributed from the center to the peripheral of each wafer were measured. It was found that the Cu surface roughness increased rapidly as the current density was increased above 40 mA/cm². The roughness data increased at a much slower rate when the current density was kept below 35 mA/cm². The shear strengths of each group of Cu studs were measured and the data are plotted in Fig. 3. The shear strength remained the same among all four groups. The examination of the fracture surface showed that all the failures were located at the interface between the electroplated Cu and the sputtered layers. This result suggested that the initial adhesion of Cu UBM layer was not affected by Cu electroplating current density. However, the reliability behaviors after thermal aging were different for different sample groups.

Stencil Printing: The nickel bumps were plated on the aluminum pads using the electroless Ni plating solution based on the sodium hypophosphite. The chemical reaction is auto-catalytic on Ni [8]

Fig. 3. Shear strength of Cu studs.

TABLE II
AL PADS AND Ni UBM SURFACE ROUGHNESS

	Ra (Å)	Std (Å)
1 st zincated Al	2600	300
2 nd zincated Al	780	120
Ni on 1 st zincated Al pad	480	50
Ni on 2 nd zincated Al pad	64	15

Due to the aluminum's high affinity for oxygen, the aluminum pads were rapidly covered with an oxide layer which impeded the formation of a metal-to-metal bonds and had to be activated by the zincation process. The zincation process was conducted by immersing the wafers into an alkaline zincation solution. The basic net reactions were the dissolution of aluminum and the deposition of zinc

The single zincation process included sodium hydroxide degrease, nitride acid etch and one zincation. For the double zincation process, the wafers were dipped into 50% volume HNO₃ after the first zincation and then were immersed into zincation bath for the second time.

Table II lists the roughness data of aluminum surfaces after two zincation processes and Ni bumps based on the two pretreatments. The aluminum pad surface after the single zincation pretreatment was rougher than that treated by the double zincation pretreatment. We also found that the Ni bumps surface morphology depended strongly on the zincation pretreatment condition. The SEM micrograph revealed that the zinc film on the single zincated aluminum pads consisted of zinc particles of various sizes. Large "isolated" zinc particles were observed on the single zincated Al pads. Fig. 4 shows the microstructures of Ni bumps plated on the single and double zincated Al pads. For the double zincation pretreated samples, the Ni grain sizes were less than 1 μm , whereas for the single zincation pretreated samples the Ni grain sizes were in the range of 5 μm to 10 μm . The shear test of Ni bumps was performed. To prevent the shear head from skipping over the Ni bump surface, Ni bumps of 15- μm height were plated. The shear height was set to be 5 μm and the shear speed was 100 $\mu\text{m/s}$. For samples by the single zincation pretreatment, the shear strength was 145 MPa. For those

Fig. 4. (a) Ni UBM by single zincation process. (b) Ni UBM by double zincation process.

Fig. 5. (a) Shear fracture of Ni bump by single zincation. (b) Shear fracture of Ni bump by double zincation.

by the double zincation pretreatment, the shear strength value was 127 MPa. D. A. Hutt *et al.* reported different results in [4]. The discrepancy could be due to the different composition in zincation baths. In our experiment, the zincation solution prepared from ZnO and NaOH was used for both zincation pretreatments. The SEM micrographs of shear fractures are shown in Fig. 5. For the double zincated samples, the fractures occurred at the interface between the aluminum and the silicon dioxide layer. For the single zincated samples, the failures occurred at the aluminum and nickel interface. Although the failure modes are different, both the single and double zincation pretreatment provided sufficient adhesion of Ni bumps to aluminum pads. As we shall present later, the zincation process has a more significant impact on the Ni bumps surface morphology than on Ni bumps shear strength.

B. Relation Between IMC Growth and UBM Microstructures

Electroplating: SEM micrographs of solder bump cross sections of SR-1 and SR-4 sample groups are shown in Fig. 6(a) and (b), respectively. There is a distinct Cu-Sn IMC layer reaction region between the solder and the Cu UBM at 600 h aging time for both sample groups. The white gray region near the solder is Cu_6Sn_5 and the dark gray region adjacent to the UBM is Cu_3Sn as identified by EDX analysis. It is reported that the Cu_6Sn_5 is formed during reflow [9]. A second intermetallic layer of Cu_3Sn was observed between Cu_6Sn_5 and Cu at the 50 h aging time point in SR-1 and SR-2 samples. The mean thickness of each IMC layer was measured by the optical microscopy with an imaging processing system. The thickness of the IMC layers versus aging time at 150 °C is plotted in Figs. 7 and 8. A linear relationship between the thickness of the IMC

Fig. 6. (a) Cross section of SR-1 after 600 h aging and (b) cross section of SR-4 after 600 h aging.

Fig. 7. Cu_3Sn thickness versus time.

Fig. 8. Cu_6Sn_5 thickness versus time.

layer and the square root of time can be established according to the parabolic growth rate law: $d = \sqrt{Dt}$ where D is the diffusion coefficient; d is the thickness of IMC and t is the aging time. Figs. 7 and 8 suggest the ratio of Cu_3Sn to the total intermetallic layer thickness depending on the Cu stud microstructure. The growth rate of Cu_3Sn was the slowest for the roughest group SR-4 while the growth rate of Cu_6Sn_5 was the fastest for this group. The Cu_6Sn_5 layer thickness in SR-4 samples grew so rapidly that it reached 80% of total IMC thickness after 800 h of aging. The intermetallic layer growth kinetic is described by the Arrhenius equation

$$D = D_0 \exp\left(-\frac{Q}{RT}\right)$$

Fig. 9. Arrhenius plots for the growth of the total Cu-Sn IMC layers.

Fig. 10. (a) Ni bump microstructure of group S. (b) The Ni bump microstructure of group D. (c) Cross section of group S at 800 h aging. (d) Cross section of group D at 800 h aging.

where

- D_0 interdiffusion constant;
- Q activation energy (J/mol) for the growth of Cu-Sn IMC layer;
- R universal gas constant;
- T absolute temperature.

The Arrhenius plots for the growth of total Cu-Sn IMC layer are shown in Fig. 9.

Other researchers have reported the growth kinetics of Cu-Sn IMC for the eutectic solder prepared by a different process [9], [10]. In our experiment, it was found that the Cu stud plating process affected the activation energy of Cu-Sn IMC growth. The activation energies were in the range of 0.78 eV to 1.14 eV for the four sample groups SR-1 to SR-4. The activation energy increased as the Cu UBM surface roughness decreased.

Stencil Printing: Two layers of IMC were observed in SEM micrographs of solder bumps aged at 150 °C at 50 h thermal aging time. Fig. 10 shows the Ni bump surface morphology of Group S and Group D and the corresponding solder bump crosssections at 800 h aging time. The dark gray layer IMC

Fig. 11. (a) EDX results of IMC region I. (b) EDX results of IMC region II.

region I next to the Ni UBM was identified as Ni_3Sn_4 . The light gray IMC region II at the solder side was identified as $(\text{Au}_x\text{Ni}_{1-x})\text{Sn}_4$ ternary IMC. Fig. 11 shows the EDX results of two IMC regions. The ternary IMC is close to $(\text{Au}_{0.4}\text{Ni}_{0.6})\text{Sn}_4$ in composition. The Au-Ni-Sn ternary IMC was observed in both single and double zincated samples at all aging temperatures. However, the distributions of the formed IMC depended on the aging temperature. At 150 °C, the two IMC layers were well attached to the UBM and continuous layers of IMC were observed. However, at 120 °C, and 85 °C, the IMC growth was quite irregular and some Au-Ni-Sn IMC was distributed within the solder bulk as shown in Fig. 12. The SEM micrograph of reflowed solder bumps before thermal aging reveals that there was a thin layer of Ni_3Sn_4 but no Au ternary IMC was observed at the interface. At 50 h thermal aging time, the thickness of formed Au ternary IMC already surpassed the thickness of Ni_3Sn_4 IMC. The thickness of IMC versus aging time at 150 °C is plotted in Fig. 13. It shows that the formation of Au-Ni-Sn was quite rapid initially for both sample groups. The first 50 h showed dramatic increase of Au-Ni-Sn IMC thickness but after 50 h the growth slowed down. It was reported that the ternary $(\text{Au}_x\text{Ni}_{1-x})\text{Sn}_4$ IMC was formed by Au diffusion back to the interface and that the IMC growth rate was controlled by the diffusion rate of Au [5], [7]. In this experiment, it was further verified that the Au diffusion is the control factor of Au ternary IMC formation. Due to the Au diffusion mechanism, the UBM surface roughness became a less significant factor. Although the larger Au ternary IMC thickness was observed for the single zincated samples, the difference could be partially contributed to the slightly different deposition rate of Au during the Au immersion step. After most of the Au in the

Fig. 12. Irregular IMC growth at 120 °C after 800 h.

Fig. 13. IMC thickness versus time at 150 °C.

Fig. 14. Arrhenius plots for the growth of the Ni-Sn IMC.

solder was consumed, the growth of IMC II slowed down and eventually stopped. The growth rate of Ni₃Sn₄ showed little difference for the two sets of samples. The Arrhenius plots for the Ni₃Sn₄ growth are shown in Fig. 14. The activation energies of Ni₃Sn₄ IMC are in the range of 0.6 eV to 0.7 eV. The activation energy of (Au_xNi_{1-x})Sn₄ IMC was not measured due to Au fast diffusion rate.

C. Shear Strength Test and Failure Analysis

Five possible failure modes were identified after the shear tests. They were identified by fracture surface locating at: bulk

Fig. 15. Shear strength versus aging time at 150 °C.

Fig. 16. Shear strength versus time in thermal and humidity test.

solder (Mode I); solder and IMC surface (Mode II); IMC surface (Mode III); IMC layer (Mode IV); UBM layer (Mode V). The preferred failure mode is Mode I.

Electroplating: After thermal aging test and thermal/humidity test, the shear strength of samples with different Cu surface roughness were measured. The results are shown in Figs. 15 and 16. It was found that the shear strength of solder bump for various Cu surface conditions was not very different before 500 h aging time. The shear strength of SR-4 sample began to decrease after aging for 600 h at 150 °C, but the shear strength of other samples did not decrease much after 600 h of aging. From 600 h to 800 h aging time, the shear strength of SR-3 and SR-4 samples ranged from 10 g to 75 g, but that of SR-1 and SR-2 samples distributed from 40 g to 75 g. The reliability of SR-3 and SR-4 samples further degraded after 800 h of aging. The temperature/humidity test did not degrade the shear strength of the four sample groups with various Cu stud structures after 100 h test.

After the shear test, the fracture surfaces of samples were examined to determine the failure mode. For the sample groups with small Cu surface roughness (SR-1, SR-2), failure modes I and II occurred after 800 h of aging. The growth of Cu-Sn IMC layer did not adversely affect the reliability of solder joints prepared from SR-1 and SR-2 samples. Fig. 17(a) shows the mode I fracture surface. For the samples with the coarse Cu stud surface and the large Cu grain (SR-4), failure modes II to V were observed after the shear tests. The fracture surfaces of many samples were located at IMC surface or Cu-Sn IMC layer (failure

Fig. 17. (a) Failure mode I: fracture was inside solder for fine Cu surfaces. (b) Failure mode III: fracture was at the IMC surfaces for rough Cu surfaces.

Mode III or IV). The shear strength of Cu-Sn IMC layer became lower than that of Sn-Pb solder bumps because there were cracks and voids inside the IMC layer. The shear strengths of solder joints were determined by Cu-Sn IMC layer. Large cavities were observed on the fracture surface for those samples having a rough Cu surface as shown in Fig. 17(b). We believe the large Cu grains on the rough Cu surface caused these cavities. These cavities caused voids in the solder and formed continuous cracks at the IMC layer and Sn/Pb solder interface. This caused the failures at the IMC layer surface (failure mode III). The high growth rate of Cu-Sn IMC layer consumed the Cu stud quickly to form the IMC layer at the bottom of the solder bump. It caused the failure mode V. Some samples failed at the UBM and IMC interface after shear strength test. It was clear that the Cu stud microstructure determined by the Cu plating process affected the failure modes and reliability of solder joints through the increasing rate of IMC growth.

Stencil Printing: The stencil printed samples were subjected to the same shear tests. The shear test was performed to measure the shear strength after 50 h, 200 h, 400 h, and 800 h of aging time. The results are shown in Fig. 18. No significant difference was observed for the two sets of samples before 400 h of aging. The shear strengths of both sample groups were about 50 MPa. After 400 h of aging, the single zincated samples showed more shear strength degradation. However, the examination of the fracture surface indicated that all the shear test failures were of mode I Type. Because of the much lower Ni-Sn IMC growth rate compared to Cu-Sn IMC, no significant UBM consumption was observed. As a result, no mode IV and mode V failures were observed even for the rougher UBM surfaces of the single

Fig. 18. Shear strength versus aging time at 150 °C.

Fig. 19. Shear strength versus time at thermal and humidity test.

zincated samples after 800 h of aging. Thermal and humidity tests were also performed. Similar shear strength values were observed for the two sets of samples as shown in Fig. 19.

Young-Doo Jeon *et al.* reported that the brittle property of Ni_3Sn_4 and the growth of Kirkendall voids caused brittle fractures [3]. Zequn Mei *et al.* reported that the main cracked area was located between Au-Sn IMC and Ni-Sn IMC due to poor adhesion of two layers and the cracks occurred between Ni-Sn IMC and Ni UBM due to weak interface between phosphorous rich layer and Ni-Sn layer [6]. In our experiment, although all the failure sources including phosphorous-rich layer were examined, no brittle fractures directly related to these sources were observed for both sets of samples. Instead, the property of solder near IMC region had more impact on the solder joint failure modes. For samples aged at 85 °C and 120 °C, there was no significant difference in the shear strength between two sets of samples even after 400 h of aging. The shear strength was determined by the properties of eutectic solder. For the samples aged at 150 °C, more degradation of shear strength was observed for the single zincated samples after 400 h of aging, although for both sample groups, the shear fractures occurred at solder as stated before. This phenomenon can be explained by the formation of Pb-rich solder layer during IMC growth. The formation of the IMC $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ and Ni_3Sn_4 consumed Sn in the solder bulk and caused depletion of Sn from the solder near the UBM. Because of the weaker strength of Pb-rich phase of solder, the shear strength became lower. The lower shear strength of single zincated samples may be due to the thicker ternary IMC and more Sn depletion in the solder layer. After all the Au was consumed, the growth of both IMC layers and Pb-rich solder layer slowed down and eventually stopped. The

Fig. 20. Illustration of typical fracture structure after thermal aging.

Fig. 21. SEM cross-sectional view of the shear fracture of the double zincated sample with excessive gold immersion after 1000 h of aging.

shear strength became stable. The duration of this process depended on the amount of Au deposited. The typical shear fracture structure is illustrated in Fig. 20. It was also found that the excessive amount of Au caused thicker IMC. If the IMC was thick enough and the IMC-solder interface was close to shear height, the failure mode may switch to mode III or mode IV. The SEM cross-sectional view of the shear fracture of the double zincated sample with excessive gold immersion after 1000 h of aging is shown in Fig. 21. The Ni UBM roughness does not significantly affect the IMC growth rate. This makes the process control easier.

IV. CONCLUSION

The UBM process and its relation to UBM microstructure and IMC growth for the electroplating process and stencil printing process were investigated. The following conclusions can be drawn from this study.

- 1) The Cu UBM surface roughness is controlled by Cu plating current density. To obtain good uniformity and reliability, the plating current density should be kept at less than 40 mA/cm^2 .
- 2) The total Cu-Sn IMC thickness increased with the increased Cu UBM surface roughness. The activation energy for the total IMC growth is in the range of 0.78 eV to 1.14 eV.
- 3) The shear strength and failure mode after thermal aging test is affected by the Cu UBM microstructures. The shear strength of solder bumps with fine Cu surface was determined by the solder properties, whereas that with rough surface was determined by the IMC layers properties.
- 4) The Ni UBM surface roughness depends on the Al pads pretreatments. Single zincation pretreatment produces rougher UBM surface and larger Ni grain size. Both single and double zincation pretreatment process provides adequate adhesion of the UBM to the Al layers.
- 5) The Au-Ni-Sn ternary IMC thickness depends on the amount of Au deposited (over the Ni layer) and the growth rate depends on the Au diffusion in the solder. The Ni UBM surface roughness is not a critical factor. The activation energy of Ni_3Sn_4 IMC growth is 0.6 eV to 0.7 eV.
- 6) The shear strength and failure mode after thermal aging test are not affected by the UBM surface roughness if the Au amount is the same. No interfacial fractures between Ni/ Ni_3Sn_4 , Ni_3Sn_4 /Au-Ni-Sn and Au-Ni-Sn/solder were observed.

REFERENCES

- [1] J. H. Lau, *Flip Chip Technologies*. New York: McGraw-Hill, 1996.
- [2] G.-W. Xiao, P. C. H. Chan, A. Teng, J. Cai, and M. M. F. Yuen, "Effect of Cu stud microstructure and electroplating process on intermetallic compounds growth and reliability of flip-chip solder bump," *IEEE Trans. Compon. Packag.*, vol. 24, no. 4, pp. 682–690, Dec. 2001.
- [3] Y.-D. Jeon and K.-W. Paik, "Studies on Ni-Sn intermetallic compound and P-rich Ni layer at the electroless nickel UBM-solder interface and their effects on flip chip solder joint reliability," in *Proc. 51th Electronic Components Technology Conf.*, 2001, pp. 1326–1332.
- [4] D. A. Hutt, C. Liu, P. P. Conway, D. C. Whalley, and S. H. Mannan, "Electroless nickel bumping of aluminum bondpads-Part I: Surfaces pretreatment and activation," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 1, pp. 87–97, Mar. 2002.
- [5] A. Zribi, L. Zavalij, P. Borgesen, A. Primavera, G. Westby, and E. J. Cotts, "The kinetics of formation of ternary intermetallic alloys in Pb-Sn and Cu-Ag-Sn Pb-free electronic joints," in *Proc. 51th Electronic Components Technology Conf.*, 2001, pp. 687–692.
- [6] Z. Mei, M. Kaufmann, A. Eslambolchi, and P. Johnson, "Brittle interfacial fracture of PBGA packages soldered on electroless nickel /immersion gold," in *Proc. 48th Electronic Components Technology Conf.*, 1998, pp. 952–961.
- [7] C. E. Ho, R. Zheng, G. L. Luo, A. H. Lin, and C. R. Kao, "Formation and resettlement of $(\text{Au}_x\text{Ni}_{1-x})\text{Sn}_4$ in solder joints of ball-grid-array packages with the Au/Ni surface finish," *J. Electron. Mater.*, vol. 29, no. 10, pp. 1175–1181, 2000.
- [8] W. Riedel, *Electroless Nickel Plating*. Stevenage, UK: Finishing Publications Ltd., 1991.
- [9] H. D. Blair *et al.*, "Manufacturing concerns of the electronic industry regarding intermetallic compound formation during the soldering stage," in *Proc. IEEE/CPMT Int. Electronic Manufacturing Technology Symp.*, Austin, TX, Oct. 1996, pp. 14–16.
- [10] C. K. So and Y. C. Chan, "Reliability studies of surface mount solder joints- effect of Cu-Sn intermetallic compounds," *IEEE Trans. Compon. Packag. Technol.*, vol. 19, no. 1, pp. 134–141, Mar. 1996.

electronic packaging.

Jing-Feng Gong received the B.S. degree from the Department of Information and Electronics, Zhejiang University, Hangzhou, China, in 2000, and the M.S. degree from the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Hong Kong, China in 2003, where he is currently pursuing the Ph.D. degree.

His current research interests are integrated MEMS sensors, passive components integration, high-frequency semiconductor devices, and elec-

Philip C. H. Chan (SM'00) was born in Shanghai, China. He received the B.S. degree (with highest honors) in electrical engineering from the University of California at Davis, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign.

He was an IBM Postdoctoral Fellow and a Visiting Assistant Professor in electrical engineering with the University of Illinois. He joined Intel Corporation, Santa Clara, CA, in 1981 as a Senior Engineer in the Technology Development Computer-Aided Design Department. Later, he became a Principal Engineer and Senior Project Manager. He has the corporate responsibility for circuit simulation tools, VLSI device modeling, and process characterization. In 1990, he transferred to the Design Technology Department, Microproducts Group. While there, he led a team of engineers that defined and developed a CAD system to design multi-chip module products. This effort led to the first functional 486 based multi-chip module at Intel. He joined the Hong Kong University of Science and Technology in April 1991 as a Reader. He became a Professor in 1997. He served as the Director of Undergraduate Studies, the founding Director of Computer Engineering Program, the Associate Dean of Engineering, and the Acting Head and then Head of the Department of Electrical and Electronic Engineering until 2002. He was also the Director of the Microelectronic Fabrication Facility. He is also the Director of the Advanced Electronic Packaging Laboratory where he initiated the research in flip-chip technology. He became the Dean of Engineering in September 2003. His research interests include microelectronics devices, circuits, integrated sensors, and electronic packaging.

Guo-Wei Xiao received the B.Eng. and M.Eng. degrees in electronic engineering from Xi'an Jiaotong University, Xi'an, China, in 1990 and 1997, respectively, and is currently pursuing the Ph.D. degree in the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Hong Kong.

He was with the Department of Electronic Engineering, Xi'an Jiaotong University, as a Lecturer from 1995 to 1998. His research interests include advanced electronic packaging and semiconductor manufacturing technologies, reliability issues, and sensor materials.

Ricky S. W. Lee (SM'00) received the Ph.D. degree from Purdue University, West Lafayette, IN, in 1992.

Currently, he is Associate Professor of mechanical engineering and Director of the Electronic Packaging Laboratory, Hong Kong University of Science and Technology, Hong Kong. Ricky has published numerous technical papers in international journals and conference proceedings. He also co-authored *Chip Scale Packages*, *Microvias for Low Cost High Density Interconnects*, and *Electronics Manufacturing with Lead-Free, Halogen-Free, and*

Conductive Adhesive Materials, respectively. His research activities cover flip chip technologies, wafer level chip scale packaging, high density interconnects, solder joint reliability, and mechanics for sensors and actuators.

Dr. Lee is a Fellow of American Society of Mechanical Engineers (ASME) and the Institute of Physics (IoP).

Matthew M. F. Yuen (M'98–SM'04) received the Ph.D. degree from Bristol University, Bristol, U.K., in 1977.

He is Director of the Technology Transfer Center, Hong Kong University of Science and Technology, Hong Kong. He has extensive research experience in design and manufacturing automation. He spent four years in U.K. industry before taking up a teaching position in Hong Kong in 1979. He has provided consultancies in design and manufacturing automation, and vibration control. He has authored over 30 papers in conferences and periodicals. His research interests include intelligent CAD/CAM systems, soft object modelling, electronic packaging, rapid prototyping, vibration control, and polymer processing.

Dr. Yuen received the 1987 Edwin Walker Prize from the Institution of Mechanical Engineers, U.K.