24.5 A 0.9V 0.35μm Adapitively Biased CMOS LDO Regulator with Fast Transient Response

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Portable applications often need multiple voltages controlled by a power management IC to power up many functional blocks [1]. A switching pre-regulator is usually followed by a low dropout (LDO) regulator to provide a regulated power source for noise-sensitive blocks. The LDO regulator has to be stable for all load conditions and frequency compensation is usually needed to stabilize the regulation loop [2, 3]. The output voltage drop due to rapid and large load changes can be minimized with a fast regulation loop, such that functional blocks powered by the same LDO regulator would have low crosstalk noise.

LDO regulators with fast load transient response were demonstrated in [4] and [5]. In [4], the regulator was implemented in an advanced 90nm CMOS process and the fast feedback loop used a small 600pF filter capacitor for stability. The fast response requires a large quiescent current of 5mA to deliver a stable current of 100mA and the 10% voltage output variations were relatively large. In [5], the power PMOS pass transistor was driven by a dynamically biased super source-follower as a buffer for both stability and speed and the buffer had to operate at a voltage higher than is usually required by low-power digital circuits. The bias current of the error amplifier was fixed, and its speed and current consumption are difficult to be optimized simultaneously. The regulator also used a 10pF capacitor for compensation, which used silicon area.

A low-voltage fast transient-response LDO regulator using an inexpensive 0.25μm CMOS process is presented in this paper. It features a current-efficient adaptively biased regulation scheme using a low-voltage high-speed super current mirror and does not require a compensation capacitor (Fig. 24.5.1). It is stabilized by a low-cost low-ESR ceramic filter capacitor of 1nF. The adaptively biased error amplifier EA (M41 to M46) drives a small transmission cell, M18, to modulate the output current IOUT through a transient-enhanced super current-mirror (SCM).

The PMOS differential input stage of the EA (M41 and M46) is driven by NMOS level shifters (M45 and M47). The level shifters allow the EA to function properly at a VDD that is only 150mV higher than VOUT. The PMOS differential pair and the NMOS active loads (M45 and M47) give a ground-referenced voltage (VRR) to drive M49. The bias currents of the level shifters and the differential pair are proportional to IOUT. As IOUT increases, the outputs of the level shifters VDG and VGU decrease, which compensates for the increase of the source-gate voltages of M45 and M47. Thus, the source node of the differential pair, VS, remains constant as IOUT varies, and the EEB of the SCM that provides the bias current IBOOST to the EA will not be forced into the triode region at heavy loads. The current densities of M45 and M47 are designed to be half that of M45 such that a slightly biased current of 5mA to achieve a gains and stabilize the loop. The current sources IP1 through IP3 are essential to keep the LDO regulator active even when IOUT is zero.

For loop stability, the frequency responses of the EA and the SCM should have low phase shifts at frequencies lower than the unity gain frequency. The gain bandwidth product GBW is A0L(2πRCOUTCOUT), where A0L and R0OUT are the low-frequency open-loop gain and output resistance of the regulator (including RLOAD), respectively. With COUT = 1pF and A0L = 10, the GBW with a full load of 50mA (PLOAD = 183) for VOUT = 0.8V is a few MHz, while at light loads it could drop to a few tens of Hz. The large current gain of K = 1000 for the SCM allows the use of a small M45 in minimizing the parasitic capacitance at VRR. Due to adaptive biasing, the EA has low power consumption at light loads, and the non-dominated pole generated at VRR tracks with the GBW and the regulator remains stable as IOUT varies.

Figure 24.5.2 shows a conventional current mirror CM and the SCM. The CM achieves a high current gain by using a large transistor aspect ratio. Speed is limited by the large time constant of COUT, where COUT is the capacitance of the diode-connected input transistor M5, and C6 is the total equivalent gate capacitance of both M6 and MOUT. The proposed SCM utilizes a low-voltage transient-enhancing circuit that provides extra transient current to C6 to enhance the current mirroring speed. A very small on-chip regulator resistor, R2 = 250Ω, is sufficient to stabilize the transient-enhancing circuit. In steady state, V2 = V5 and VBOOST regulates M43 such that IBOOST = IIN = IOUT/K. If there is a rapid increase of IIN, which would reduce the drain currents of M6 and M9 quickly, M43 and M44 react with a delay by design. The sudden mismatch in the drain currents of M6 and M9 pulls VBOOST up to increase IBOOST. The node voltage V2 is then pulled down first followed by V5 due to the RC delay generated by R2 and C6. The voltage difference across R2 is amplified by M43 through M46 and pulls VBOOST further up to provide extra current such that IBOOST > IIN to compensate for the delay and to stabilize the transient-enhancing loop. A similar mechanism applies to a rapid decrease of IIN.

Figure 24.5.3 shows the frequency responses of the SCM and the CM for comparison. At a light load of ILOAD = 1mA, the CM has a phase shift of 60° at 100kHz, but the SCM has the same phase shift at a much higher frequency of 2MHz. The minor gain peaking at 2.5MHz is caused by the <90° phase margin of the transient-enhancing loop. It occurs at a frequency much higher than the GBW of the regulation loop and the overall stability of the regulator is not affected. At a full load of ILOAD = 50mA, both the bandwidths of the SCM and the CM are larger due to the increase in the bias currents. The CM has a phase shift of 60° at 2MHz, and the SCM has the same phase shift at 8MHz, which is high enough for the regulator to be stabilized with a 1pF filter capacitor.

Figure 24.5.4 shows the measured load transient response. The load current is switched between 0mA and 50mA with rise and fall times of 10ns. No overshoot is observed for the switching from 50mA to 0mA, as the regulation loop has a large bias current initially, giving a high unity gain frequency. For the switching from 0mA to 50mA, a minor undershoot occurs due to the low bias current at IOUT = 0mA. However, the total output voltage variation is only 6.6mV (0.73%/p,p) and is much smaller than those in [4] and [5].

Figure 24.5.5 shows the measured quiescent current IQ versus IOUT. At a high ILOAD, IQ increases linearly, demonstrating a working adaptive-biasing scheme. At no load, the EA and the SCM are kept active by a total bias current of only 4.04μA. Figure 24.5.6 tabulates all the important parameters of the proposed regulator in comparison with those of [4] and [5]. The die micrograph is shown in Fig. 24.5.7. The regulation loop occupies only 24% of the total active area.

References:
Figure 24.5.1: LDO regulator.

Figure 24.5.2: A conventional current mirror and the super current mirror with the low-voltage transient-enhancing circuit.

Figure 24.5.3: Frequency response of the super current mirror.

Figure 24.5.4: Measured load transient response.

Figure 24.5.5: Measured $I_I$ versus $I_{LOAD}$ and current efficiency ($I_{LOAD}/I_I$) versus $I_{LOAD}$.

Figure 24.5.6: Performance summary and comparison with previously published LDO regulators.

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Figure 24.5.7: Die micrograph.