Analysis of Switching-Loss-Reduction Methods for MHz-Switching Buck Converters

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Abstract – Numbers of switching-loss-reduction methods recently proposed for MHz-switching buck converters are thoroughly investigated. From a theoretical perspective, switching loss is found to be effectively minimized by adapting the width rather than the turn-on voltage of power transistors of a buck converter. From a practical point of view, the advantage of adapting the width of power transistors becomes diminished. The amount of switching loss minimized by adapting the width of power transistors is also found to be reduced and approached to that minimized by adapting the turn-on voltage of power transistors as technology to fabricate the buck converters is continuously down scaled.

I. INTRODUCTION

Buck converters (BCs) are widely used in mobile systems to efficiently provide voltage conversion in step-down manner, which are necessary as supply voltage of mobile-application circuits is continuously reduced but battery voltage is more or less the same. Different techniques [1-6] have been proposed to minimize the conduction loss contributed by the body diode of rectifying transistor. However, mobile systems such as cellular phones and personal digital assistants are often in standby mode that makes BCs operating in the light-load region, where the dominant power loss is no longer the conduction loss but the switching loss. As MHz-range switching frequency is essential to the use of compact off-chip inductor and capacitor for BC-size minimization, switching loss is inevitably increased so that BC light-load efficiency is significantly degraded. Pulse-frequency modulation (PFM) is a well-known method to effectively reduce switching loss. Still, BCs with PFM is subjected to a load-dependent output spectrum, which can create problems to noise-sensitive circuits such as Bluetooth and Wi-Fi modules that are widely integrated into nowadays mobile systems. Recently, different methods [7-12] are proposed to improve light-load efficiency of BCs operated at constant switching frequency in MHz range. Width switching (WS) in [7-8], dynamic loss control in [9], or segmented output stage in [10], are proposed to reduce switching loss with very similar mechanism, in which power transistor is partitioned into different segments. Segments or partial width of power transistor is adaptively conducted in small load current. Another method is to adaptively reduce the

turn-on voltage of power transistor in small load current. Examples are low-voltage-swing gate drive (LVSGD) in [11] and gate charge modulation in [12].

To yield better understanding on aforementioned methods, the switching-loss-reduction ability of the WS and the LVSGD should be thoroughly investigated. The paper is organized as following. Section II describes the models used to calculate different power losses of a BC. The switching-loss-reduction ability of the WS and the LVSGD is investigated in Section III. Finally, a conclusion is given in Section IV.

II. POWER-LOSS MODELS OF BUCK CONVERTERS

Fig. 1 Schematic of a generic buck converter with different elements for power-loss analysis.

Fig. 1 shows the schematic of a generic BC where different elements are included for power-loss analysis. It is well known that conduction loss (CL) is the dominant loss in heavy load current. CL is caused by current flowing through the on-resistance of both power PMOS transistor (M_{PP}) and power NMOS transistor (M_{PN}), the series resistance of inductor (R_L), the series resistance of output capacitor (R_C), and the body diode of M_{PN} (D_B) during dead-time. To simplify the following analysis, it is assumed that loss of D_B is greatly minimized by either one of methods suggested in [1-6]. Moreover, loss of

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the R_L and the R_C is ignored as it only depends on the choice of external components but not the loss reduction methods. The CL of M_{PP} (P_{CLPP}) and the CL of M_{PN} (P_{CLPN}) are expressed in equation (1) and (2)

$$P_{CLPP} = I_{RMS_PP}^2 \cdot R_{PP} \quad (1)$$

$$P_{CLPN} = I_{RMS_PN}^2 \cdot R_{PN} \quad (2)$$

where the root-mean-square current of M_{PP} (I_{RMS_PP}) and M_{PN} (I_{RMS_PN}) can be found in [12]. On-resistance expressions of M_{PP} (R_{PP}) and M_{PN} (R_{PN}) are shown in (3) and (4)

$$R_{PP} \approx \frac{1}{\left[\mu_{PP} C_{OX} \frac{W_{PP}}{L} (V_{DD} - V_{PSS} - V_{THPP}) \right]} \quad (3)$$

$$R_{PN} \approx \frac{1}{\left[\mu_{PN} C_{OX} \frac{W_{PN}}{L} (V_{NDD} - V_{THPN}) \right]} \quad (4)$$

where V_{DD} is the BC input voltage. V_{NDD} and V_{PSS} are gate-drive level to turn on M_{PN} and M_{PP} , respectively. In conventional control, V_{NDD} is set to V_{DD} and V_{PSS} is set to zero. C_{OX} is oxide capacitance per unit area and L is channel length of M_{PP} and M_{PN} . μ_{PP} , W_{PP} , and V_{THPP} and μ_{PN} , W_{PN} , and V_{THPN} are mobility, width, and absolute value of threshold voltage of M_{PP} and M_{PN} , respectively.

As load current of BC is reduced, the CL is also scaled down. However, switching losses (SLs) is not scaled with the load current, which is the reason that SLs are the dominant loss in middle-to-light load current. There are two major SLs. The first one is the power (P_{SLX}) consumed to charge the switching node capacitance (C_X), which is contributed by the drain-to-body diode-capacitance of M_{PP} and M_{PN} , and the converter IC and the off-chip inductor package capacitance. As mentioned before, it is assumed no loss contributed by D_B . It means that energy stored in the C_X can be fully transferred to the output capacitor of BC during dead-time. Another SL is the power consumed by the buffers used to switch the gate of M_{PN} (P_{SLPN}) and M_{PP} (P_{SLPP}). These losses are expressed in equation (5), (6), and (7)

$$P_{SLX} = 0.5 C_X f_s V_{DD}^2 \quad (5)$$

$$P_{SLPN} = C_{TPN} f_s V_{DD} V_{NDD} \quad (6)$$

$$P_{SLPP} = C_{TPP} f_s V_{DD} (V_{DD} - V_{PSS}) \quad (7)$$

where f_s is the switching frequency of BC. C_{TPN} and C_{TPP} are the total capacitance of the power NMOS buffer and the power PMOS buffer, correspondingly. They are shown in equation (8) and (9)

$$C_{TPN} = \frac{W_{PN} L C_{OX} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} \quad (8)$$

$$C_{TPP} = \frac{W_{PP} L C_{OX} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} \quad (9)$$

where β is the tapering factor and n is the total number of stage of both the power NMOS buffer and the power PMOS buffer.

III. EFFECTIVENESS ANALYSIS

Both the WS and the LVSGD reduce the power used to switch the M_{PP} and the M_{PN} . However, these two methods inevitably raise conduction loss as the on-resistance of M_{PP} and M_{PN} is increased. To enable a fair comparison between these methods on the switching-loss-reduction ability, it is necessary to enable the WS and the LVSGD with the same level of conduction loss. This can be done by purposely equating the on-resistance of M_{PP} and M_{PN} in both the WS and the LVSGD. It means that for the given V_{NDD} and V_{PSS} used in the LVSGD, there are equivalent transistor widths for the M_{PN} and the M_{PP} (W_{PN_WS} and W_{PP_WS}) so that the value of R_{PP} and R_{PN} in both the WS and the LVSGD are the same. The relationships between V_{NDD}/V_{SPP} and W_{PN_WS}/W_{PP_WS} are given in equation (10) and (11)

$$W_{PN_WS} = \frac{W_{PN} (V_{NDD} - V_{THPN})}{V_{DD} - V_{THPN}} \quad (10)$$

$$W_{PP_WS} = \frac{W_{PP} (V_{DD} - V_{PSS} - V_{THPP})}{V_{DD} - V_{THPP}} \quad (11)$$

By substituting (10) into (6) and (8), and (11) into (7) and (9), the switching loss of BC with the WS (P_{SLPN_WS} and P_{SLPP_WS}) can be calculated and expressed in (12) and (13)

$$P_{SLPN_WS} = \frac{W_{PN} (V_{NDD} - V_{THPN})}{(V_{DD} - V_{THPN})} \times \quad (12)$$

$$\frac{LC_{OX} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} f_s V_{DD}^2$$

$$P_{SLPP_WS} = \frac{W_{PP} (V_{DD} - V_{PSS} - V_{THPP})}{(V_{DD} - V_{THPP})} \times \quad (13)$$

$$\frac{LC_{OX} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} f_s V_{DD}^2$$

Switching loss of BC with the LVSGD ($P_{\text{SLPN_LVSGD}}$ and $P_{\text{SLPP_LVSGD}}$) can also be calculated and expressed in (14) and (15)

$$P_{\text{SLPN_LVSGD}} = \frac{W_{\text{PN}} L C_{\text{OX}} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} \times f_s V_{\text{DD}} V_{\text{NDD}} \quad (14)$$

$$P_{\text{SLPP_LVSGD}} = \frac{W_{\text{PP}} L C_{\text{OX}} [\beta^{(n+1)} - 1]}{\beta^n (\beta - 1)} \times f_s V_{\text{DD}} (V_{\text{DD}} - V_{\text{PSS}}) \quad (15)$$

Since the switching loss expressions such as $P_{\text{SLPN_WS}}$ and $P_{\text{SLPP_WS}}$ are very similar, and more importantly they share the same power-loss mechanism, only the switching loss of M_{PN} (e.g. $P_{\text{SLPN_WS}}$ and $P_{\text{SLPN_LVSGD}}$) is used to simplify the following analysis. By comparing $P_{\text{SLPN_WS}}$ and $P_{\text{SLPN_LVSGD}}$ for a given R_{PN} , the switching-loss-reduction ability of the WS and the LVSGD can be fairly compared. Fig. 2 shows the plot of $P_{\text{SLPN_WS}}$ and $P_{\text{SLPN_LVSGD}}$ as a function of R_{PN} . Values used in the above equations are shown in Table I. It can be clearly observed in Fig. 2 that the WS has higher ability to reduce the switching loss of BC compared to the LVSGD. At 1-Ohm on-resistance of M_{PN} , the switching loss of BC with WS is almost ten times smaller than that with the LVSGD. To understand what is the major factor that makes the WS outperformed the LVSGD, equations (12) and (14) have been carefully studied. It is found that the finite threshold voltage of power transistor M_{PN} is the root of this phenomenon. Fig. 3 shows the plot of $P_{\text{SLPN_WS}}$ and $P_{\text{SLPN_LVSGD}}$ as a function of V_{THPN} . It can be clearly observed in Fig. 3 that the $P_{\text{SLPN_WS}}$ is increased and approached to the $P_{\text{SLPN_LVSGD}}$ as the V_{THPN} is reduced. This also implies that the use of advanced technology, which mostly has shorter minimum channel length and smaller threshold voltage, make the amount of switching loss reduced by the WS to be decreased and approached to the one reduced by the LVSGD.

Another important point to note is that width of power transistor is very difficult, if not impossible, to be continuously scaled with the load current of BC in practical implementation. As mentioned before, the practical way to scale the width of power transistor is done by partitioning the whole power transistor into different segments [7-10]. The number of segment to be conducted is then adaptively reduced with decreased load current. Therefore, switching loss of BCs with the practical WS shows stair-like relationship with the load current as illustrated in Fig. 4

Fig. 2 Plot of switching loss of BC with the WS and the LVSGD as a function of on resistance of M_{PN} .

TABLE I
VALUES USED IN EQUATIONS

μ_{PN} (cm^2/Vs)	300
C_{OX} (F/m^2)	$5\text{e-}3$
W_{PN} (mm)	50
L (μm)	0.35
V_{DD} (V)	2.7
V_{THPN} (mV)	500
f_s (MHz)	4
β	10
n	4

Fig. 3 Plot of switching loss of BC with the WS and the LVSGD as a function of threshold voltage of M_{PN} .

Fig. 4 Relationship between switching loss and load current under both theoretical and practical WS.

IV. CONCLUSION

In this work, the recently proposed methods to reduce switching loss of MHz-switching BCs such as the WS and the LVSGD are thoroughly investigated. It is found that the WS can have much higher switching-loss reduction compared to the LVSGD when the width of power transistors of a BC can be continuously scaled with the load current. As adapting the width of power transistor with load current is very difficult, the switching-loss-reduction ability of WS becomes diminished in practical implementation. Moreover, the amount of switching loss minimized by the WS is found to be reduced and approached to the one minimized by the LVSDG when the threshold voltage of power transistors is reduced. Therefore, it is suggested that the LVSGD should be used in BCs with advanced technology where threshold voltage of transistors is usually small. The WS can be used in BCs where the power transistors have large threshold voltage (e.g. high-voltage process).

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