**5.4 0.9mW 7GHz and 1.6mW 60GHz Frequency Dividers with Locking-Range Enhancement in 0.13µm CMOS**

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Frequency dividers are key components for frequency synthesis in wireless and wireline communication systems. Among different types of frequency dividers, LC-based injection-locked frequency dividers (ILFDs) feature high-frequency operation at low power consumption, but their locking range is quite narrow due to the high-Q nature of the resonator. Recently, design techniques to enhance the locking range of ILFDs have been reported. Injection into two coupled LC oscillators [1] and sandwiched injection into two identical LC oscillators [2] are proposed, but these techniques are suitable for dividers with quadratic outputs. Inductive-peak and transconductance-enhancement techniques [3, 5] are also used but they require extra inductors and thus larger chip area. In this paper, a simple but effective technique is presented to improve the locking range of ILFDs without extra inductive components while consuming low power.

Figure 5.4.1(a) shows the schematic of a conventional ILFD, and its behavioral model is shown in Fig. 5.4.2(a). The differential pair \( M_2 \) and \( M_3 \) acts as a single-balanced mixer, to mix the feed-back output voltage \( V_c \) at frequency \( f_c \) with both the dc current \( I_{dc} \) and the ac current \( I_{ac} \) at frequency \( 2\omega \) provided by the tail transistor \( M_r \), where the current ratio \( I_{dc}/I_{ac} \) is defined as the injection ratio \( \eta \). \( I_{dc} \) and \( I_{ac} \) are the mixing products of \( I_{dc} \) and \( V_c \), \( V_c \) and \( V_c \), with the conversion coefficients \( k_1 \) and \( k_2 \), respectively. Due to the high selectivity of the LC tank, only the current components at frequency \( f_0 \) are considered at the mixer's output. Two conditions need to be satisfied for the divider to work properly. First, the loop gain needs to be at least unity, which is easy to satisfy for the ILFD as long as \( I_{dc} \) is large enough for self-oscillation. Second, the total phase shift in the loop needs to be zero. Consequently, as shown in Fig. 5.4.2(a), the phase shift \( \phi \) needs to be compensated to induce the phase shift \( \beta \) from the LC tank at the operation frequency \( f_0 \). Due to the high-Q of the LC tank, as \( \omega \) moves away from \( \omega_0 \), \( I_{dc} \) increases rapidly and \( I_{ac} \) needs to be increased accordingly. From the phasor diagrams in Fig. 5.4.2(b), the maximum \( I_{ac} \) is given by \( \sin(\beta I_{ac}/I_{dc}) \), which is proportional to \( k_2/k_1 \). Due to the mixing property, the conversion coefficient \( k_2 \) is always smaller than \( k_1 \). which limits the maximum achievable \( I_{ac} \). As a result, increasing the injection ratio \( \eta \) is critical for the improvement of the phase condition and thus the locking range.

Given a fixed input swing the injection ratio \( \eta \) can be increased by reducing the bias gate voltage of \( M_1 \) to operate it in Class-C mode instead of Class-A mode. However, the \( V_{dd} \) size of \( M_1 \), would need to be increased rapidly to maintain the biasing current, which would result in large parasitic capacitance at the drain node and limit the effective achievable injection ratio [6]. A simple solution to improve the injection ratio is to steer away some of the dc current from \( M_2 \) and \( M_3 \) by connecting a current source \( V_{pp} \) to the common-source node as shown in Fig. 5.4.1(b). The current bleeding also reduces the overdrive voltage of \( M_2 \) and \( M_3 \) and thus improves the switching of the single-balanced mixer. The current source can be simply implemented by a PMOS with a constant gate bias voltage. Moreover, as shown in Fig. 5.4.1(c), the injection ratio can be improved further by applying the ac input signal to the gate of the bleeding PMOS \( M_1 \), instead of a constant gate voltage. As such, the PMOS transistor acts not only to reduce the dc current but also to inject more ac current to the divider. Since the bleeding current is reused to bias the PMOS transistor, no extra power is required. Figure 5.4.2(b) shows the differences on the phasor diagrams between the conventional ILFD and the proposed injection-enhanced ILFD. By increasing \( I_{dc} \) and reducing \( I_{ac} \), the phase condition and thus the locking range are significantly improved. Finally, as shown in Fig. 5.4.1(c), ac coupling is implemented for both \( M_2 \) and \( M_3 \) to enable the divider to operate at a lower supply voltage.

Two dividers with the same topology shown in Fig. 5.4.1(c) are designed and fabricated in a 0.13µm CMOS process (\( V_{dd}=0.4V \), \( V_{pp}=0.3V \)). The first divider is designed to operate around 7GHz, in which the transistors \( M_2 \) and \( M_3 \) are biased in Class-AB mode to provide the required bias current with small W/L sizes. The shunted dc current through \( M_1 \) is designed as large as possible to maximize the trans-conductance of \( M_2 \) while leaving enough dc current through \( M_2 \) and \( M_3 \) for the divider's self-oscillation, which is necessary to guarantee the ILFD to operate with a lower power compared to that of a Miller divider. To further demonstrate the feasibility of the proposed technique for wide range of frequencies and applications, a second divider is designed to operate around 60GHz. Figure 5.4.3 shows the die micrographs of the two proposed ILFDs, occupying active areas of 0.033mm² and 0.0165mm², respectively.

Figure 5.4.4 shows the measured input sensitivity curves of the 7GHz ILFD under different bias conditions. Operated with a 1.1mA current from a 0.8V supply and a 0dBm input signal, the divider measures a locking range of 12.8% from 6.65 to 7.56GHz when the PMOS is turned off. An improved locking range of 33.6% from 6.02 to 8.45GHz is measured when the PMOS is turned on. As the supply voltage is increased to 1.2V, the divider measures locking ranges of 14.6% from 6.52 to 7.55GHz and of 45.2% from 5.45 to 8.63GHz when the PMOS is disabled and enabled, respectively. When the input power is 0dBm and the supply voltage is 1.2V, the maximum locking range with the PMOS enabled is up to 50%, which is about 3x larger than that without the PMOS.

Figure 5.4.5 shows measured input sensitivity curves of the 60GHz ILFD. With 0dBm input power and drawing 2mA from a 0.8V supply, the divider measures a locking range of 6.5% from 59.93 to 63.97GHz with the PMOS disabled. When the PMOS is enabled, the locking range of the divider is extended to 59.6 to 66.96GHz. The improvement in the locking range for the 60GHz divider is smaller as compared to that of the 7GHz divider, because the parasitic capacitance contributed by the PMOS becomes more significant at higher input frequencies. Inductive peaking could be applied to cancel the parasitic capacitance and improve the locking range further at the expense of larger chip area. Figure 5.4.6 summarizes the measured performance of the two presented ILFDs and compare the results with that of the reported state-of-the-art wide-locking-range dividers.

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**References:**


Figure 5.4.1: (a) Conventional LC ILFD, (b) current-bleeding LC ILFD, and (c) the presented injection-enhanced frequency divider.

Figure 5.4.2: (a) Behavioral model of LC ILFD, and (b) phasor diagrams of the current injection into the LC tank.

Figure 5.4.3: Die micrographs of the ILFDs.

Figure 5.4.4: Measured sensitive curves and locking ranges of the 7GHz ILFD under different bias conditions.

Figure 5.4.5: Measured sensitive curves and locking ranges of the 60GHz ILFD under different bias conditions.

Figure 5.4.6: Performance summary and comparison.