A Single-Chip UHF RFID Reader in 0.18 μm CMOS Process

Wenting Wang, Shuzuo Lou, Kay W. C. Chui, Sujiang Rong, Chi Fung Lok, Hui Zheng, Hin-Tat Chan, Sau-Wing Man, Howard C. Luong, *Senior Member, IEEE*, Vincent K. Lau, and Chi-Ying Tsui

Abstract—A single-chip UHF RFID reader that integrates all building blocks—including an RF transceiver, IQ data converters, and a digital baseband—is implemented in a 0.18 μm CMOS process. A high-linearity RX front-end and a low-phase-noise synthesizer are proposed to handle the large self-interferer, which is a key challenge in the reader RX design. Highly reconfigurable mixed-signal baseband architecture for channel-selection filtering is proposed to achieve power optimization for multi-protocol operation with different system dynamic ranges and data rates. The reader dissipates a maximum power of 276.4 mW when transmitting maximum output power of 10.4 dBm and receiving the tag's response of -70 dBm in the presence of -5 dBm self-interferer while occupying 18.3 mm².

Index Terms—Radio-frequency identification, reader, reconfigurable, RFID, self-interferer, single-chip, tag, transceiver.

I. INTRODUCTION

RADIO-FREQUENCY identification (RFID) systems operating in the UHF band from 860 to 960 MHz have the potential of extremely low cost, data transfer robustness, high efficiency and high throughput. In such systems, the readers provide energy to the passive tags and exchange information with tags by the propagation of electromagnetic waves in the far-field region.

Most of the existing RFID readers are built out of discrete components, which are bulky, expensive, and consume large power. A single-chip direct-conversion reader implemented in 0.18 μm SiGe BiCMOS is reported in [1], which achieves good performance but consumes 1.5 W. Another single-chip direct-conversion reader is demonstrated in 0.18 μm CMOS technology [2], which focuses on linearity rather than noise and only consumes 160 mW, but the high RX sensitivity requirement in the absence of the self-interferer and multi-protocol ability are not fully addressed. This work describes a single-chip dual-conversion CMOS RFID reader fully integrating a complete transceiver with the digital baseband.

Manuscript received December 26, 2007; revised March 28, 2008. Published July 23, 2008 (projected). This work was funded by the grant ITP/027/07LP from the Hong Kong R&D Center for Logistic Supply Chain Management with support from Hong Kong Innovation and Technology Fund.

W. Wang and H. Zheng were with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology. They are now with Broadcom, Irvine, CA 92618 USA.

S. Lou was with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology. He is now with the Applied Science and Technology Research Institute (ASTRI), Hong Kong.

K. W. C. Chui, S. Rong, C. F. Lok, H.-T. Chan, S.-W. Man, H. C. Luong, V. K. Lau, and C.-Y. Tsui are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong (e-mail: eeluong@ee.ust.hk).

Digital Object Identifier 10.1109/JSSC.2008.925601

Making use of the unique system specifications, the transceiver is optimally designed so that high sensitivity and low noise are the main focus in the listen mode while high linearity becomes the main objective in the talk mode. In addition, the analog and digital baseband are designed to be highly reconfigurable in terms of architecture and power consumption for multi-protocol environments and different data rate. The reader is designed based on EPC Class 1 Generation-2 protocol [3] from 860 to 960 MHz. Fabricated in a 0.18 μm CMOS, the reader consumes a maximum power of 276.4 mW (136 mW from the TX, 124.3 mW from the RX, 7.4 mW from synthesizer, and 8.67 mW from digital baseband) and occupies a die area of 18.3 mm² [4].

The paper is organized as follows. First, the unique system features and challenges of the passive UHF RFID system are briefly reviewed in Section II together with existing solutions and their limitations. The transceiver specification and the proposed transceiver architecture are described in Section III. Section IV presents the circuit implementation of the proposed transceiver. Finally, experimental results are discussed and summarized in Section V.

II. RFID SYSTEM FEATURES AND CHALLENGES

In passive RFID systems, the readers (interrogators) generate and transmit signals to serve not only as interrogation signals but also as a power supply source to the tags (transponders). A tag captures the energy it receives from a reader to supply its own power and then executes commands sent by the reader. As defined in EPC Gen-2 protocol [3], in each round of communication, the reader is required to transmit a high-power continuous-wave (CW) signal to supply energy to the passive tags, which inevitably couples to the receiver's input as a strong self-interference, which may lead to saturation of the receiver. Furthermore, due to the tags' backscatter scheme, the self-interferer locates right in the middle of the receiving band. The large power difference between the strong CW signal and the tags' weak response presents a major challenge to the reader's RX design. Moreover, the phase noise generated from the CW would significantly increase the RX noise floor and thus degrade its sensitivity.

To filter out the blocker and local oscillator (LO) phase noise, the TX output is utilized as RX LO in [5] which results in correlated phase noise between the RX LO and the blocker. Therefore, it is claimed that the increase of the noise floor due to the blocker from the transmitter would be folded to DC and eventually rejected by a DC offset cancellation circuit. However, in practice, the TX's power amplifier (PA) usually has a large and

variable output power, which inevitably requires variable-gain and variable-phase buffers or complicated interface between the down-mixer input and the PA output. The resultant noise mismatches can easily deteriorate the effectiveness of the cancellation technique. Moreover, routing the high power PA output close to the low-noise amplifier (LNA) impairs the isolation between RX and TX due to unavoidable substrate coupling. The LO leakage and frequency pulling issues are also expected to be much worse.

It would be most effective if the self-interferer and its noise floor can be filtered at the RF input to maintain the RX linearity and sensitivity. With RF frequency of 900 MHz and notch bandwidth of about 500 kHz, such an RF filter would require a quality factor Q of more than 1800. Existing RF design techniques fail to provide such a highly selective, low-noise, and tunable RF filter. A cancellation scheme is proposed in [5], where the blocker rejection is achieved through a combination of two RF paths. Nevertheless, the effectiveness of this technique highly depends on the phase and gain mismatches between the blocker and the desired signal, which is virtually impossible to control well unless some intelligent detection and calibration scheme is employed.

Due to the limitations of the cancellation techniques, most of the RFID readers choose to live with the self-interferer. Zero-IF architectures are typically used so that the self-interferer is down-converted to DC and can be removed by the DC-offset-cancellation circuit. LO with low phase noise and RX front-end with high linearity as well as limited gain are typically implemented [1], [2]. This paper adopts these similar strategies to deal with the self-interferer. However, dual-conversion zero-IF2 architecture is adopted to alleviate the problem with DC offset cancellation and $1/f$ noise. Furthermore, two separate antennas are adopted for the TX and the RX in this work to achieve maximum isolation of around 35 dB [6] to allow maximum output power from the TX for maximum communication distance. In addition, layout floorplan is carefully done to minimize the on-chip substrate coupling from the PA to the LNA.

In addition to the self-interferer, in the dense-reader environment, interference can come from nearby working readers, which causes adjacent channel interference and further degrades the signal-to-interference ratio. Moreover, the capability to handle multiple protocols makes the adjacent interference rejection ability even more challenging. As an example, in Europe CEPT multi-channel regulatory environment [7], 10 channels of 200 kHz each in the range 865.6 to 867.6 MHz are allocated. Readers talk in even-numbered channels, and tags backscatter in the odd-numbered ones. Consequently, the adjacent channel interference is expected to appear around 400 kHz offset. On the other hand, in North America, the transmitter's channel bandwidth is 500 kHz according to FCC rule [8]. Therefore, a multi-protocol reader that can be reconfigured to dynamically minimize the power consumption while meeting all the multiple-protocol requirements presents another major challenge. In this paper, a reconfigurable mixed-signal baseband architecture which focuses on power optimization for different system bandwidth and interference scenarios is proposed and demonstrated.

III. RFID TRANSCEIVER SPECIFICATION AND PROPOSED ARCHITECTURE

The transceiver specification is studied and derived based on EPC Gen-2 standard [3], CEPT protocol [7] and FCC regulation [8].

A. Receiver

The RX operation mode is separated into *listen* mode and *talk* mode [7]. Prior to each transmission by a reader, its receiver shall switch to the *listen* mode and monitor a selected sub-band. Any signal detected by the receiver in excess of the threshold level shall indicate that another device already occupies the sub-band. Only when a vacant band is detected, the reader is allowed to switch to *talk* mode. Consequently, in the *listen* mode, the reader only receives without transmitting, i.e., the high-power CW to supply power to the passive tag does not exist. On the other hand, in the *talk* mode, the reader is ready to communicate to the tags, and therefore needs to transmit the CW during each interrogation. In other words, the unique operation necessitates different requirements of the reader in each mode. According to [3] and [7], the target RX sensitivity in the *listen* mode is -90 dBm at the highest data rate of 640 kb/s, while in the *talk* mode, it is not explicitly specified. The reader is allowed to operate at a lower sensitivity in the *talk* mode. As such, most of the RX specifications are derived for the *listen* mode.

The receiver bandwidth (BW) is determined by the data rate, coding, and modulation schemes adopted for the tag-to-reader communication link in EPC Gen-2 specification. Power spectrum density (PSD) of FM0 and Miller coding has a DC-free characteristic with the signal BW of about twice the link frequency (LF) [9]. Therefore, it is optimal and desirable that the reader RX would have a tunable bandwidth to accommodate for different data rates. In this way, both the RX sensitivity and selectivity can be optimized.

Another key parameter is the minimum required signal-to-noise ratio (SNR) for reliable decoding. A reader digital baseband behavior model is developed to perform the system simulation for all the required coding and modulation schemes. The detailed algorithm is described in Section IV. For a targeted BER of 10^{-3} , SNR is at about 11 dB for ASK FM0 and 9 dB for ASK Miller subcarrier with M being 2, respectively. Since PSK modulation has 3 dB gain, the minimum SNR for PSK is 8 dB for FM0 and 6 dB for Miller subcarrier, respectively.

The RX IIP3 is calculated based on the blocking profile in the *listen* mode as specified in CEPT regulation. The two tones with the same magnitude of -35 dBm are assumed to locate at adjacent and alternate adjacent channels, whose frequency spacing is the system channel bandwidth. Their intermodulation product should be no larger than input referred noise floor of -98 dBm, and for a given desired signal of -87 dBm and SNR_{out} of 11 dB, $\text{IIP3} > -35 + (101 - 35)/2 = -2$ dBm.

Given the same blocking profile, SNR and BW, the phase noise and the spur of the frequency synthesizer are derived to be -123 dBc/Hz at 1 MHz offset and -63 dBc, respectively.

B. Transmitter

In North America, the UHF band is governed by FCC rule, Part 15, Section 247 regulations. Adopting spread-spectrum

TABLE I
SPECIFICATION OF THE PROPOSED RFID READER

System Specification	Value	
Frequency range	860MHz-960MHz	
RX		
Receiver bandwidth	80KHz to 1.28MHz	
BER	10^{-3}	
$\text{SNR}_{\text{out} _{\text{max}}}$	11dB	
Listen mode sensitivity	−90dBm	
Listen mode noise figure @ 640kbps	12dB	
IIP3	−2dBm	
Maximum gain	95dB	
Frequency synthesizer		
Phase noise	−123dBc/Hz @ 1MHz	
Spur	−63dBc	
Frequency resolution	100KHz	
TX		
Transmitter bandwidth	200 KHz for Europe	500 KHz for North America
Output power (w/o external PA)	8dBm	
Output power tuning range	20dB	
Output power (w external PA)	20dBm-27dBm	
ACPR	30dB	
Process	0.18μm CMOS	

techniques, the maximum channel bandwidth is 500 kHz with an effective isotropically radiated power (EIRP) of 4 W. In Europe, the ETSI EN 302 208-1 rule provides a channel spacing of 200 kHz and maximum effective radiated power (ERP) of 2 W. 20 dB output power tuning range is designed which is of special importance in the RFID system. For short distance applications, the output power should be reduced which can greatly relax the RX linearity performance. One important feature of the reader's transmitter is that the pulse-interval-encoding (PIE) format adopted in the R $\Rightarrow$ T communication link has strong energy at DC. Therefore, normal AC-coupling interface between the building blocks in the transmitter has to be avoided.

Table I summarizes all the specifications for the proposed RFID reader. Fig. 1 shows the block diagram of the proposed single-chip RFID reader's transceiver, which utilizes IQ down-conversion to support PSK modulation and IQ up-conversion for single-sideband (SSB) ASK generation. The RX employs dual-conversion zero-IF2 architecture and makes use of the DC-free coding scheme in EPC Gen-2 standard to remove both the DC offset and the down-converted CW signal from the TX. Compared with the direct-conversion architecture which is normally adopted for existing RFID readers, the proposed architecture has less problems with LO leakage and frequency pulling because LO1, LO2, and RF frequencies are all located far from each other. The LO signals are designed and generated from a fractional-N frequency synthesizer, and by choosing $f_{\text{LO2}} = f_{\text{LO1}}/2$, the image frequency of the first down-conversion at about 300 MHz is rejected by 40 dB thanks to the bandpass

characteristics of antenna [6] and of the LNA, which eliminates the need for an image-rejection filter and facilitates high level of integration. The LNA is bypassed in the *talk* mode in order to avoid saturation with the self-interferer because in the *talk* mode the RX sensitivity is actually dominated by the phase noise of the blocker rather than the thermal noise. The LNA is turned on in the *listen* mode to enhance the RX's *listen* mode sensitivity. An on-chip clock generator is embedded to make use of the synthesizer's outputs to provide multiple and variable clocks to all the building blocks in the analog and digital basebands, including RX switched-capacitor (SC) channel-selection filter (CSF), $\Sigma\Delta$ ADC, DAC, and digital baseband.

IV. CIRCUIT IMPLEMENTATION

A. Frequency Synthesizer

A low-power fractional-N frequency synthesizer is fully integrated in the reader system [10]. By properly distributing the capacitance between drain and source of a transformer-feed-back (TF) VCO [11], the modified VCO exhibits enhancement in the tank's Q factor as well as benefits from the noise filtering of even-ordered harmonics. The combined effects of these two mechanisms bring about 2-4 dB improvement in the phase noise compared with the original TF-VCO. A third-order 2-bit single-loop $\Sigma\Delta$ modulator is designed to add negligible noise to the loop and to optimize the phase noise and the power consumption. The LO1 achieves a phase noise of -126 dBc/Hz at 1 MHz offset, which is limited by the low quality factor of the on-chip transformers.

Fig. 1. Block diagram of the proposed RFID reader transceiver.

Fig. 2. Schematic of the proposed linearized LNA.

B. Receiver Front-End

1) *LNA*: Although bypassed in the *talk* mode, the LNA still has a very challenging linearity requirement in the *listen* mode, especially in the dense-reader mode to deal with large interferences caused by adjacent working readers. The schematic of the highly linear LNA with a proposed linearization technique [12] is shown in Fig. 2.

For a differential pair, the IM3 mainly originates from the nonlinearity of the active devices' I - V characteristic. The small-signal output current around the quiescent bias point can be expressed by a Taylor series expansion as

$$i_d = g_1(v_g - v_s) + g_2(v_g - v_s)^2 + g_3(v_g - v_s)^3 + \dots \quad (1)$$

where g_i represents the i th-order transconductance coefficient of the input device, and v_g and v_s are the gate and source voltages. Analysis reveals that for two input tones located at ω_1 and ω_2 with equal magnitude of A , if a low-frequency second-order

intermodulation (IM2) current i_{inj} given by (2) is injected to the bias transistor M3, the intrinsic third-order intermodulation term IM3 generated by the LNA can be canceled without affecting the gain.

$$i_{inj} = 2 \left(\frac{-3g_1g_3}{4g_2} + \frac{3}{2g_2} \right) A^2 \cos(\omega_1 - \omega_2)t. \quad (2)$$

If the injected current has a non-zero phase mismatch, IM3 cancellation is not effective. However, the phase matching requirement is not difficult to achieve because the injected signal is located at low-frequency ($\omega_1 - \omega_2$). Thus, this technique is applicable for wide range of systems because the injected signal is not related to the RF frequency but the channel spacing ($\omega_1 - \omega_2$). Furthermore, effective cancellation over wide range of input power may be achieved because the injected signal is tracking the input signal power, as shown in (2).

A simple IM2 injection circuit shown in Fig. 2 is designed which only consumes an extra current of 0.2 mA but suppresses the IM3 by 17 dB. pMOS transistors are used to achieve the negative coefficient g_2 required for cancellation. All the noise generated by the squaring circuit is injected at the common-source node and is rejected by the differential pair's high common-mode rejection ratio.

One potential problem with the proposed technique is that the injected IM2 may leak to the output and degrade IIP2 in the presence of device mismatches. However, this is not a problem for narrowband applications like RFID in which IM2 tones are located completely outside of the signal bands.

The LNA impedance matching is achieved by connecting 70- Ω resistors in parallel with the gates of the input transistors. In both the *listen* and *talk* modes, the termination resistor dominates the input impedance, making the input impedance independent of the mode setting. From simulations, 70- Ω termination achieves about -14 dB S11 with better NF as compared with 50- Ω one.

2) *Down-Conversion Mixer*: In the *talk* mode with LNA passed, the down-mixer's linearity, in particular the input P_{-1dB}

Fig. 3. Schematic of the proposed two-stage IQ down-mixer.

becomes the most stringent to deal with due to the presence of a large blocker. Although passive mixers exhibit superior linearity and are implemented in [2], an active mixer with targeted gain of 9 dB is crucial to suppress noise contribution from later stage in the *listen* mode with LNA bypassed. As a result, a two-stage stacking active mixer is adopted to balance the conflict requirements on gain, noise and linearity. Fig. 3 shows the combined schematic of the two-stage IQ down-mixers for the RX. The first mixer employs MOSFET operating in triode region (M1a and M1b) as the input transconductance for good linearity. The channel length of the input transistor is optimized for maximum linearity and minimum flicker noise without introducing significant capacitive loading to the LNA. The two mixer stages are interfaced in the current mode by stacking the second-stage IQ mixers on top of the outputs of the first mixer. The signal current is divided into two paths and then mixed with IQ LO signals. This current mode interfacing technique has much better linearity performance compared to the traditional cascade interfacing in voltage mode. The double converted signal current is then folded with the current sources (M3a–d and R1a–d) and the cascode transistor M4a–d. The folded-cascode structure increases the output voltage swing and minimizes the signal-dependent voltage variation on the drain nodes of M3a–d.

C. Reconfigurable Analog Baseband

To cope with different baseband bandwidths and to optimally adapt the power consumption under different interference scenarios for multi-protocol operation, a highly reconfigurable analog baseband is implemented in terms of architecture, clock frequency, baseband channel bandwidth, and power consumption. The baseband is composed of an active trap,

an anti-aliasing filter (AAF), a switched-capacitor channel selection filter (CSF), and a $\Sigma\Delta$ ADC.

1) *Active Trap*: An active-trap following the down-mixer relaxes the linearity of baseband stages by providing partial channel selection and synthesizing a notch at the alternate adjacent frequency but keeping the signal band intact [13]. For the proposed multi-protocol reader, the active trap has to furnish a wide tuning ability to reject interference at different offset frequencies. Therefore, two simple traps in [13] are connected together by a tunable resistor R_t which is implemented by a 5-bit switched-resistor array. Together with the bias current changing, notches of about 12 dB at different frequencies can be generated.

2) *Anti-Aliasing Filter (AAF)*: The AAF employs a G_m -C architecture which is converted from a fifth-order elliptic ladder filter prototype as shown in Fig. 4. The order is over-designed in order to meet the worst-case anti-aliasing requirement with enough margins as well as to provide partial channel selection. The transconductor core is shown in Fig. 4. G_m linearity is first ensured by the use of grounded amplifier, which forces a linear relationship between the input voltage and current through node A+ and A-. Therefore, the transconductance stems primarily from the Z_x (impedance between node A+ and A-) with the effective G_m equal to $1/Z_x$. In this work, Z_x is a 5-bit switched-resistor array (SRA) for discrete tuning. Good linearity is preserved over the whole tuning range of about 11 times from 145 kHz to 1.612 MHz without affecting the DC operation point. In addition, all-digital bit control provides an easy interface with the baseband circuitry without a need for A/D or D/A converters. Since the input g_m -cell of the filter dominates the noise performance but does not affect the filter's transfer characteristic, a separate g_m -cell with simple source-degeneration architecture is adopted to minimize the

Fig. 4. Schematic of the anti-aliasing filter.

Fig. 5. Architecture of the $\Sigma\Delta$ ADC.

noise while providing moderate linearity. Variable-gain stages are added before and after the filter core to achieve variable gains from 3 dB to 55 dB in 1 dB steps.

3) *Channel-Selection Filter*: Since the RFID system features a relatively low bandwidth but wide dynamic range, switched-capacitor (SC) circuit is a suitable choice. Besides, bandwidth tuning can be easily achieved by changing the clock frequencies which makes it attractive for the proposed multi-protocol baseband. The CSF is composed of a first-order filter followed by a biquadratic filter. Because the clock frequency is chosen to be the same as that of the ADC with an oversampling ratio of 16, the gain and offset compensation technique [14] is applied to relax the gain requirement of the opamp for low power consumption. As a result, a simple current mirror opamp with DC gain of 50 dB is sufficient. A 12-dB variable gain is imple-

mented in the first-order low-pass filter by a 2-bit switched-capacitor array. The biquad architecture in [15] is adopted which breaks all direct charge transfer paths between the two opamps and synthesizes transmission zeros without global feedback to significantly improve the operation speed.

4) $\Sigma\Delta$ ADC: To meet the maximum dynamic range (DR) requirement of 70 dB for the maximum bandwidth of 1.28 MHz, MASH 2-1-1 $\Sigma\Delta$ ADC architecture with moderate oversampling ratio (OSR) of 24 is chosen as shown in Fig. 5. Due to stringent linearity requirement, a one-bit comparator is used to avoid the need for dynamic-element-matching (DEM) technique to linearize the feedback D/A converter. In addition, this architecture reduces the complexity and nonidealities such as offset and hysteresis of the comparator contributed to the overall ADC at the expense of relatively high-gain amplifier, particularly in the first integrator.

Fig. 6. Block diagram of the proposed reconfigurable baseband.

The coefficients of the analog and digital part of the proposed $\Sigma\Delta\text{M}$ are

$$\begin{aligned} \text{Analog : } [a_1 \ a_2 \ a_3 \ a_4 \ a_5 \ a_6 \ b_1 \ b_2 \ b_3] \\ = [1/4 \ 1/2 \ 1 \ 1/4 \ 1 \ 1/4 \ 1/4 \ 1/4 \ 1/4] \end{aligned} \quad (3)$$

$$\text{Digital : } [c_1 \ c_2 \ c_3] = [-1 \ 2 \ 2]. \quad (4)$$

To suppress both the quantization noise leakage and the harmonic distortion, folded-cascode OTA with the gain-boosting is designed to enhance the DC gain to 80 dB. Gain-boosting is not necessary and not used in the OTAs for the last two stages since the noise contributions are greatly suppressed by the gain of the first stage in the $\Sigma\Delta$ loop. At the same time, the capacitors are scaled down to reduce the settling time requirement and hence the power.

5) *Reconfigurability*: To determine a systematic way to reconfigure the baseband, theoretical analysis has been performed. The target is to minimize the total power consumption subject to the constraints on interference and baseband bandwidth. For the CSF, noise contribution from the switches and opamps are included. For simplicity, the following assumptions are made in the analysis: 1) noise sources are uncorrelated; 2) opamp gain is infinitely large; 3) parasitic capacitance can be negligibly small. For a given noise level and settling accuracy, the power consumption of the analog CSF can be expressed in the form of

$$P_{\text{CSF}} = \frac{nkTf_bV_{\text{DD}}}{v_{\text{tot,in}}^2}\gamma \quad (5)$$

where f_b is the signal bandwidth, n is the order of the CSF, γ is a factor that depends on the opamp and filter architecture, V_{DD} is the supply voltage, and $v_{\text{tot,in}}$ is the input referred noise. Therefore, the power of CSF is proportional to f_b and inversely proportional to the noise power. Similar analysis is performed on the $\Delta\Sigma$ ADC by assuming that the thermal noise dominates the dynamic range [16]. The ADC power is found to be proportional to f_b and its DR. At the system level, the order of the channel-selection filter and ADC's dynamic range can be traded

off with each other. Following the calculations in [17], with the system sensitivity P_{sen} of -90 dBm, adjacent channel blocker P_{blo} of -35 dBm, and the ADC's noise level 20 dB lower than the thermal noise, the dynamic range specification of ADC is related to the filter attenuation by

$$\begin{aligned} \text{DR}_{\text{ADC}} &= P_{\text{blo}} - \rho - P_{\text{sen}} + 20 + 11 \\ &= (-35) - \rho - (-90) + 31 = 86 - \rho \end{aligned} \quad (6)$$

where ρ is filter attenuation. As a consequence, the baseband total power can be expressed and optimized under different combinations of CSF and ADC for a target sensitivity and interference. The analysis shows that for the RFID system, to cope with different electromagnetic environments, mixed-mode channel-selection approach is the most power-efficient to handle large interference while bypassing the analog filter and using only digital channel selection is favorable for relaxed interference scenario. As such, the proposed baseband is reconfigured into 2 modes. In the first mode, the ADC is sampled at $\text{OSR} = 24$ or $\text{OSR} = 16$ with CSF bypassed. In the second mode, the ADC and CSF are both sampled at $\text{OSR} = 16$, as shown in Fig. 6. Moreover, due to the intrinsic linear dependency of the power on the bandwidth f_b , the clock frequency of CSF and ADC are adaptively varied, and the analog bias currents are adjusted accordingly so as to optimize the total power for different data rates and bandwidths.

D. Transmitter

1) *DAC and TX Filter*: TX behavior simulation shows that an 8-bit DAC is sufficient for the PIE-encoded ASK data. A current-steering DAC is designed with five thermometer MSBs and three binary-weighted LSBs. A two-dimensional centroid-switching sequence is implemented in the thermometer portion. To minimize the systematic error, a symmetrically-located current source in each of the four quadrants of the matrix is selected simultaneously. A two-stage row-column decoding logic is implemented for the thermometer-control signals which only requires simple NAND and NOR gates with two or three inputs.

Fig. 9. Block diagram of the digital baseband.

Fig. 10. Die micrograph of the RFID reader.

the PIE-encoded packet is $4\times$ up-sampled with respect to the period of $T_{\text{ari}}/4$ and interpolated by a raised-cosine filter to obtain a transmitted spectrum within the mask. The 8-bit IQ data are then input to the current-steering DACs.

The receiver digital baseband consists of three main sections: a decimation filter which decimates the signals from the $\Sigma\Delta$ ADC and removes both noise-shaped and out-of-band interference, an automatic gain control (AGC) which detects the received signal power and generates gain-control signals for the analog VGA, and a front-end processor. The decimation filter, which consists of a comb filter and a low-pass FIR filter, can be reconfigured to decimate from $64\times\text{LF}$ or $96\times\text{LF}$ to $4\times\text{LF}$, where LF is the tag-to-reader backscatter link frequency [3]. The front-end processor is responsible for detecting the bit boundary (timing synchronization) and start of the packet (frame synchronization) in the backscattered reply from a tag and for recovering FM0 or Miller-subcarrier encoded bits. As the modulation scheme used in the tag transmitter is ASK or PSK, the matched filter in the synchronization and bit decoding processing can do the job without the need of a dedicated baseband demodulator. The two synchronizations use running windows to calculate the correlated value in the preamble frame. If the correlated value is bigger than a certain threshold, the bit/frame boundary is found. For bit decoding, the correlated value compared with the threshold value is used to determine if a bit-0 or

bit-1 is received. The algorithm employed can achieve bit-error rate (BER) of 10^{-3} at signal-to-noise ratio (SNR) of about 11 dB for FM0 and SNR at least 2 dB lower for Miller-subcarrier.

V. MEASUREMENTS

The RFID reader is fabricated in a 0.18 μm CMOS process with six metal layers. Fig. 10 shows the die micrograph of the reader, which occupies a chip area of 2.9 mm $\times$ 6.3 mm including all the pads and 17.4 mm² without pads.

RF frequency from 772 MHz to 1.05 GHz with a resolution of 25 kHz is generated by the fractional- N frequency synthesizer. The phase noise is measured to be -76 dBc/Hz in-band, -110 dBc/Hz at 200 kHz offset and -126 dBc/Hz at 1 MHz offset at a center frequency of 880 MHz. The reference spur of -84 dBc and worst case fractional spur of -70 dBc are measured. The synthesizer consumes 7.4 mW from 1 V supply [10].

The ADC peak SNR and SNDR are 70.6 dB and 68.6 dB at the maximum sampling frequency of 61.44 MHz, respectively. To demonstrate the reconfigurability, measurements are done with three different bandwidths of 200 kHz, 640 kHz, and 1.28 MHz. Fig. 11 depicts the measured SNR and SNDR versus input signal level at OSR = 16 (low DR scenario) and OSR = 24 (high DR scenario) for all three cases. The measured dynamic ranges at OSR = 16 and OSR = 24 are 67 dB and

Fig. 11. Measured SNR/SNDR versus input level at different BW and OSR (M).

Fig. 12. Measured linearity of RX front-end in the *listen* and *talk* modes.

72 dB, respectively, in all cases while the power is tuned from 7.4 mW to 39.8 mW.

Sampled at about 5 MSamples/s clock rate, the DAC measures a SFDR of better than 67 dB while consuming 2 mW from 1 V supply. The measured differential and integral linearity errors are $\text{DNL} < \pm 0.48 \text{ LSB}$ and $\text{INL} < \pm 0.45 \text{ LSB}$.

The RX front-end linearity is the most critical to handle the self-interferer which will be greatly attenuated after down-converted to DC and has less effects on the RX baseband. As shown in Fig. 12, for *listen* mode operation with LNA turned on, the RX front-end measures $P_{-1\text{dB}}$ of -9.4 dBm and IIP3 of 0 dBm . In *talk* mode with LNA bypassed, the RX front-end measures $P_{-1\text{dB}}$ of 3.5 dBm , IIP3 of 18 dBm . The $P_{-1\text{dB}}$ in both cases are dominated by the down-mixer. The whole RX measures $P_{-1\text{dB}}$ of -14.5 dBm and out-of-band IIP3 of 3 dBm in smallest gain setting.

The RX measures a total gain from 10 dB to 94 dB. The 3 dB bandwidth can be tuned from about 80 kHz to 1 MHz. The worst-case RX sensitivity is -90 dBm for ADC output SNR of 11 dB for all the bandwidths from 80 kHz to 1.28 MHz. By adding a single tone of -5 dBm at the carrier frequency to the

Fig. 13. ADC output spectrum with and without adjacent channel interference. (a) $f_b = 1.28 \text{ MHz}$. (b) $f_b = 200 \text{ kHz}$.

LNA input, the impact of the self-interferer is measured. The RX output noise floor shows a 20 dB increase, which corresponds to a RX sensitivity of -70 dBm .

To illustrate the RX reconfigurability, a big adjacent channel interferer is added on top of the small desired signal. Define δ the power difference of the interference and minimum detectable signal at RX input. Fig. 13(a) shows the ADC output spectrum with highest data rate of 640 kb/s, to maintain an in-band SNR of 11 dB, δ is 55 dB. Fig. 13(b) shows when the data rate is reduced, the RX bandwidth is smaller, the adjacent channel interferer is also closer. The phase noise of the interferer raises the in-band noise floor, so to maintain a same output SNR of 11 dB, δ reduces to 50 dB. Such testing is repeated for three data rates with CSF turned on and ADC's OSR of 16. In Fig. 14, the measured ADC output SNR with a -90 dBm intended signal at RX input is plotted versus the adjacent channel interference power. As discussed above, negligible sensitivity degradation for adjacent interferers up to -37 dBm is observed excepted for the low data rate case. For narrow band, the impact of the close-in phase

Fig. 14. ADC output SNR versus adjacent channel interference.

Fig. 15. Maximum adjacent channel interference (upper curve) and RX total power consumption (lower curve) versus data rates.

noise of the adjacent channel interference can be improved by increasing the ADC's OSR to 24 as shown in Fig. 14.

Through the interferer rejection testing, the baseband is re-configured into the two modes for the three selected BWs. Note that in the digital channel-selection mode, two different OSRs are possible which results in a total of three configurations. Fig. 15 plots the maximum interference and receiver power consumption versus the data rate. At small data rate, the impact of the interferer phase noise is significant, so the maximum adjacent channel interference is small. When CSF is on, the performance is the best at the cost of the largest power consumption. In total, the receiver power can be varied from 48 mW to about 106 mW with LNA bypassed, showing significant programmability. Power can also be minimized when blocker rejection is relaxed. With CSF bypassed and the ADC's OSR set to 16, the baseband consumes only 33 mW at 640 kb/s, which is about half of the maximum power at the same bandwidth.

(a)

(b)

Fig. 16. Measured TX spectrum for DSB-ASK with $T_{\text{ari}} = 12.5 \mu\text{s}$ (a) without digital baseband and (b) with digital baseband.

TABLE II
POWER BREAKDOWN OF THE PROPOSED RFID READER TRANSCEIVER

Building blocks		Supply voltage (V)	Power consumption (mW)
RX	LNA	1.8	18.7
	Down-mixer	1.8	24.6
	Active trap (IQ)	1.8	1.2
	AAF (IQ)	1.8	9
	CSF (IQ)	1.8	31
	ADC (IQ)	1.8	39.8
RX total			124.3
Frequency synthesizer		1	7.4
TX	DAC (IQ)	1	4
	Up-mixer	1.8	28.8
	RF-VGA	1	103.2
TX total			136
Baseband		1.8	8.67

The transmitter measures an output-referred 1-dB-compression point of 10.4 dBm without external PA and better than 30 dBm with an external PA (EMPOWER 1075-BBM3Q6A3E). The sideband rejection ratio is -53.6 dBc. The TX output spectrum is measured by storing the baseband PIE encoded data into the pattern generator and inputting into the DAC. Illustrated in Fig. 16(a), the output spectrum for DSB-ASK with $T_{\text{ari}} =$

TABLE III
MEASURED PERFORMANCE SUMMARY OF THE PROPOSED RFID READER

Operating Frequency		860MHz to 960MHz
RX		
Listen mode	Front-end P1-dB	-9.4dBm
	Front-end IIP3	0dBm
	Noise figure (BW=1.28MHz)	12dB
	RX sensitivity	-90dBm
Talk mode	Front-end P1-dB	3.5dBm
	Front-end IIP3	18dBm
	RX sensitivity (-5dBm self-interferer)	-70dBm
IIP3 (small gain)		>3dBm
P1-dB		>-14.5dBm
Gain range		10dB to 94dB
baseband bandwidth		80KHz to 1MHz
Output SNR		11dB
IQ gain mismatch		0.6dB
IQ phase mismatch		3°
Output DC offset voltage		4mV
TX		
Side-band rejection		-53.6dBc
Output P-1dB w/o PA		10.4dBm
Output P-1dB w/ PA		>30dBm
OIP3 w/o PA		18dBm
OIP3 w/ PA		>50dBm
ACPR		30dBc
Frequency Synthesizer		
Phase noise @ 880MHz		-110dBc/Hz @ 200KHz -126dBc/Hz @ 1MHz
Fractional spur		<-70dBc
Reference spur		<-84dBc
Frequency resolution		25KHz
Frequency tuning range (LO1)		530MHz to 700MHz
Technology		0.18 μ m 1P-6M CMOS
Die size		18.3mm ²

12.5 μ s satisfies the transmit mask for dense-interrogator environments. The transmitter consumes a maximum power of 136 mW. Finally, the reader's transceiver is also measured with the TX baseband. As shown in Fig. 16(b), the output shows more noise mainly due to reduced driving capability of the on-chip interface and increased delay compared with the almost ideal pattern generator, so it can only marginally fulfill the spectrum mask requirement for EPC Gen2 dense-reader mode.

The measurement of the reader receiver with the baseband is not available due to an incorrect scaling coefficient in the decimation filter. As such, field-programmable gate array (FPGA) prototyping (Xilinx Virtex-II xc2v1500) is performed to verify the functionality and performance. With an 11 dB SNR at the RX ADC output, the BERs are measured to be

TABLE IV
PERFORMANCE SUMMARY OF SINGLE-CHIP RFID READERS

	Ref [1]	Ref [2]	Ref [5]	This work
Process	0.18 μ m SiGe BiCMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Integration level	RF, BB for physical layer	RF, BB modem, MPU, memory	Reader front-end	RF, BB
LO phase noise	-116@200K -144@3.6M	-87@100K -120@1M	N/A	-110@200K -127@1M
front-end P-1dB (low gain mode)	11dBm	8dBm	N/A	3.5dBm
Sensitivity w/o blocker	-96dBm	N/A	N/A	-90dBm
Sensitivity w/ blocker	-78dBm @0dBm	-70dBm @0dBm	N/A	-70dBm@ -5dBm
output power	20dBm	4dBm	N/A	10.4dBm
Die size	21mm ²	23.9mm ²	2.1mm ²	18.3mm ²
Total power	1.5W	160mW	56mA@3.3V	<276.4mW

10^{-3} and 0.6×10^{-3} for ASK FM0 and ASK Miller-subcarrier ($M = 2$), respectively.

Table II shows the power breakdown of the transceiver, the RX building blocks are operated at 1.8 V because of the stringent linearity requirement. The synthesizer, DAC and PA are operated at 1 V supply for best balance between performance and power dissipation while the up-mixer is still operated at 1.8 V for high linearity. Table III summarizes the performance of the proposed RFID reader transceiver, which fulfills all the specifications. Table IV compares the proposed RFID reader with other recent published state-of-the-art single-chip readers. Compared with CMOS implementation in [2], this work focuses more on the reconfigurability, and achieves comparable linearity and higher output power.

VI. CONCLUSION

A single-chip UHF RFID reader integrating all the building blocks including a frequency synthesizer, IQ data converters and digital baseband is successfully demonstrated in 0.18 μ m CMOS technology. A high-linearity RF front-end with a linearization technique and a low-phase-noise frequency synthesizer help tackle the problem with large self-interferer in the talk mode. The reconfigurable baseband architecture is studied in detail which allows power optimization for the multi-protocol operation. The complete reader including the digital baseband meets all the specifications for EPC Gen 2 while consuming maximum power of 276.4 mW and occupies a chip area of 18.3 mm².

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Wenting Wang received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2003, and the Ph.D. degree from the Hong Kong University of Science and Technology in August 2007. Her Ph.D. research was on the integration of an UHF RFID reader system.

In December 2007, she joined Broadcom Corporation, Irvine, CA, as a staff design scientist.

Shuzuo Lou received the B.Sc. degree in microelectronics from Peking University, Beijing, China, and the Ph.D. degree in electronic engineering from the Hong Kong University of Science and Technology (HKUST), in 2002 and 2007, respectively.

From October 2007 to March 2008, he was a research associate in the Department of Electronic and Computer Engineering, HKUST. He is now with Hong Kong Applied Science and Technology Research Institute (ASTRI), Hong Kong. His research interests include CMOS RF and analog integrated

circuits.

Kay W. C. Chui received the B.Eng. degree in electrical engineering from the Hong Kong University of Science and Technology (HKUST).

He joined the Analog Laboratory of Electronic Department of HKUST in 2005. His research interest is investigating linearization techniques in RF front-ends.

Sujiang Rong received the B.S. degree in information science and electronic engineering from the Zhe Jiang University (ZJU), China, in 2003. From 2003 to 2006, he worked at Winbond Electronic Ltd. Shanghai, China, as an RFIC design engineer. In 2007, he received the M.Phil. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST). He is currently working toward the Ph.D. degree at HKUST.

His research interests include integrated frequency synthesizer, power amplifier and RF transceivers.

Chi-Fung Lok received the B.Eng. (1st Class Honors) and M.Phil. degrees in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST) in 2005 and 2007, respectively.

Since 2007, he has been with Fujitsu Microelectronics Limited, where he designs and develops analog/mixed-signal integrated circuits for system-on-chip. His current interest focuses on switched-capacitor circuits and data converters design.

Hui Zheng was born in Zhe Jiang, China. He received the B.S. degree in electronic engineering from Southeast University, Nanjing, China, in 2001. In 2001, he joined the Institute for Infocomm Research in Singapore as a Research Assistant. From 2003 to 2008, he was with the Department of Electronic and Computer Engineering at the Hong Kong University of Science and Technology, Hong Kong, where he received the Ph.D. degree in 2007.

His research interests include CMOS analog and RF integrated circuits and systems. In February 2008, he joined Broadcom Corporation, Irvine, CA, as a staff design scientist.

Hin-Tat Chan received the B.Eng. degree in electronic and communication engineering from the University of Hong Kong in 2005 and the M.Phil. degree in electrical and electronic engineering from the Hong Kong University of Science and Technology in 2007.

In August 2007, he joined Solomon Systech Limited in Hong Kong, and is currently a design engineer responsible for display driver chip design. His research interests include design and analysis of digital system, digital signal processing, communi-

cation, and mixed-signal integrated circuits.

Sau-Wing Man received the M.Phil. degree in electrical and electronic engineering from the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology (HKUST), under the supervision of Prof. Vincent K. Lau. His research projects include single-chip ASIC design for RFID passive tags, automatic gain controllers for RFID readers, 802.11a Wireless Communication System with FPGA, and Simulink Co-verification Model design for Advanced Wireless Communication Systems. His research interests include low-power VLSI design, digital baseband ASIC architecture and RTL design for wireless communications, and FPGA design and implementation.

Howard C. Luong (SM'02) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California at Berkeley in 1988, 1990, and 1994, respectively.

Since September 1994, he has been with the Electrical and Electronics Engineering faculty at Hong Kong University of Science and Technology, where he is currently a Professor. In 2001, he took a one-year sabbatical leave to work with Maxim Integrated Products, Sunnyvale, CA, on wireless products. His research interests are in RF, analog,

and mixed-signal integrated circuits and systems for wireless and portable applications. He was a coauthor of two books, *Low-Voltage RF CMOS Frequency Synthesizers* (Cambridge University Press, August 2004) and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems* (Kluwer Academic Publishers, July 2003).

Vincent K. Lau received the B.Eng. (Distinction 1st Hons.—ranked 2nd) from the Department of Electrical and Electronics Engineering, University of Hong Kong, in 1992 and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1997.

He was with the Bell Labs, Lucent Technologies, Murray Hill, NJ, during 1997–1999 and 2001–2004 as a Member of Technical Staff, and he joined the Department of Electrical and Computer Engineering, Hong Kong University of Science and Technology (HKUST) as an Associate Professor from 2004. His

major research interests include wireless communication systems (MIMO,

OFDM, CDMA, cooperative communications, cognitive radio) as well as signal processing algorithm and ASIC architecture.

Dr. Lau is currently an Editor of IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, and was a guest editor of the IEEE JOURNAL ON SELECTED AREAS ON COMMUNICATIONS (JSAC) Special Issue on Limited Feedback. He was a series editor of the Information and Communications Technologies (ICT) book series for John Wiley and Sons, as well as an editor of the *EURASIP Journal on Wireless Communications and Networking*.

Chi-Ying Tsui received the B.S. degree in electrical engineering from the University of Hong Kong, and the Ph.D. degree in computer engineering from the University of Southern California, Los Angeles, in 1994.

He joined the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology in 1994 and is currently an Associate Professor in the department. His research interests cover both design automation and design.

His current research includes designing VLSI architectures for low-power multimedia and wireless applications, developing power management circuits and techniques for embedded portable devices and ultra-low-power systems. He has published more than 100 refereed technical journal and conference papers.

Dr. Tsui received the Best Paper Awards from the IEEE TRANSACTIONS ON VLSI SYSTEMS in 1995 and IEEE/ACM ISLPED in 2007, and supervised the Best Student Paper Award of the 1999 IEEE ISCAS. He also received the Outstanding Design Awards of the IEEE ASP-DAC University Design Contest in 2004 and 2006.