Read-out Circuit Analysis For High-speed Low-noise VCO Based APS CMOS Image Sensor

Fang Tang, Amine Bermak

Hong Kong University of Science and Technology
Hong Kong, China
Email: icdetf@ust.hk, bermak@ieee.org

Abstract—A detailed read-out circuit analysis of the VCO based APS CMOS image sensor is presented in this paper. According to the mathematic analysis and simulation results, the read-out speed should be decreased when reducing the bias current. Moreover, the feature of the device gain factor and the source follower’s threshold voltage are investigated, showing important effects with respect to not only the read-out time but also the energy consumption. The proposed VCO based read-out circuit and frequency counter consist an equivalent bandpass filter. According to the transfer function analysis of this equivalent filter, the noise cancellation efficiency is jointly determined by the bias current, device gain factor and source follower’s threshold voltage, which constitute the basic principles for high-speed low-noise CMOS APS image sensor design.

Keywords—APS imager, CMOS image sensor, high speed, low noise.

I. INTRODUCTION

High-speed low-noise CMOS image sensor has gained considerable improvement over the last decade, while a number of high speed CMOS imagers are reported [1]. Moreover, high-speed low-noise camera has already been commercialized [2], which leads to several still and video applications especially in the field of biology, such as: multi-exposure high dynamic range camera [3], insect’s wing movement recorder and so forth.

In this paper, we perform the mathematic analysis about the read-out circuit of a novel VCO based CMOS APS imager, combining with some simulation results. Intuitively, the read-out speed suffers from decreased bias current of the source follower and benefits from increased device gain factor. Additionally, the source follower’s threshold voltage plays a vital role in determining the read-out speed. The energy consumption for each read-out process and the transfer function of CDS circuit are also investigated, which shows that increased read-out speed contributes to an improved performance of the noise cancellation.

This paper is organized as follows. In section II, the analysis about the read-out speed is reported. In section III, the energy consumption is discussed. In section IV, the relationship between the read-out speed and the noise cancellation is presented, while Section V concludes this paper.

II. OPERATING SPEED OF THE READ-OUT CIRCUIT

The schematic of a standard 4T APS pixel with a source follower is shown in Fig. 1, which composes the basic functional unit of a CMOS imager. It is clearly that, the charging time at the capacitor $C_T$ is much shorter than its discharging time, for the reason that the output voltage changes exponentially with time during charging and linearly during discharging [4]. Normally, shorting the column capacitor $C_T$ to ground at the beginning of each read-out phase can avoid longer settle time and as a result, the read-out time is only determined by the speed of the charging progress.

The transient function of the charging process can be described by Eq. 1 while ignoring the channel modulation effect and other non-linear effects for both the source follower and the bias current source.

$$I_B + C_T \frac{dV_{out}}{dt} = K_n(V_{in} - V_{th} - V_{out})^2$$

Above differential equation can be analytically solved as follow:

$$V_{out} = V_{in} - V_{th} - \beta \tanh \left[ \frac{K_n \beta}{C_T} t + \frac{1}{2} \ln \left( \frac{\beta + \alpha}{\beta - \alpha} \right) \right]$$

Where, $\alpha = V_{in} - V_{th} - V_{out}(0)$, $\beta = \sqrt{I_B/K_n}$ and $V_{out}(0)$ is the initial voltage of the output node.

In order to uncover the intrinsic relationship between the read-out speed and the bias current value $I_B$, Eq. 2 could be transformed as:

$$t = \frac{C_T}{K_n \beta} \left[ \tanh \left( \frac{1}{\beta} - \frac{V_{out}(0) - V_{out}}{\beta} \right) - \frac{1}{2} \ln \left( \frac{\beta + \alpha}{\beta - \alpha} \right) \right]$$

After simplification, the time $t$ is equal to:

$$t = \frac{C_T}{2K_n \beta} \ln \left( \frac{\beta + \alpha + V_{out}(0) - V_{out}}{\beta - \alpha + V_{out}(0) + V_{out}} \right)$$
In the reference paper [5], the read-out time $T_R$ is defined as ‘the time from the access transistor turning on to the output voltage $V_o$ reaching to within half a bit of its steady state value’ and therefore, the read-out speed gets benefit from reducing the bias current. However in practice, the read-out settle time is increased by reducing the bias current, which is shown from the Cadence transient simulation waveforms in Fig. 2. It is obviously that, the higher bias current, the shorter settle time and the lower output steady voltage.

In order to quantitatively calculating the read-out time, we assume that the ADC resolution is $n$-bit and the output voltage swing is $V_s$. Thus, the LSB voltage could be determined as:

$$V_{LSB} = \frac{V_s}{2^n} \quad (5)$$

For an infinite read-out time, the output voltage can be derived as:

$$V_{out}(\infty) = V_{in} - V_{th} - \sqrt{I_B/K_n} = \alpha - \beta + V_{out}(0) \quad (6)$$

Additionally, it is reasonable to define that the output enters into the steady state as long as the difference voltage $V_{\infty} - V_{out} \leq 1/2V_{LSB}$. Thus, the read-out time $T_R$ can be determined according to the following equation by replacing $V_{out}$ using $V_{out}(\infty) - 1/2V_{LSB}$:

$$T_R = \frac{C_T}{2K_n\beta} \ln \left(\frac{(\alpha + \beta + V_{LSB})(\alpha - \beta)}{V_{LSB}(\alpha + \beta)}\right) \quad (7)$$

For instance, the ADC resolution is 8-bit, the output voltage range is 2V and the initial voltage of the output is 0V, then the read-out time as a function of the bias current $I_B$ and the device gain factor $K_n$ can be demonstrated in Fig. 3.

It is important to state that, as $I_B$ increased, $\frac{2\sqrt{I_B/K_n+V_{LSB}}(\alpha-\beta)}{(4\beta+V_{LSB})(\alpha+\beta)}$ is decreased and then $T_R$ could be finally decreased. This trend will not be changed with different values of the device gain factor $K_n$. It should be noted that $K_n$ significantly affects the performance of the read-out circuit. Since the larger value of $K_n$, the higher read-out speed, enhancing the device gain factor can equivalently reduce the bias current, increase the output voltage swing and finally save the DC power consumption.

III. ENERGY CONSUMPTION ANALYSIS OF THE READ-OUT CIRCUIT

The total energy consumption during the read-out phase is a linear function of the integration for the source follower’s channel current $I_{DS_{SF}}$. For a given bias current $I_B$, the total energy consumption $E$ could be expressed as:


\[ E = V_{dd} \int_0^{T_R} I_{DS_{SF}} \, dt \]

\[ = V_{dd} \int_0^{T_R} I_B + V_{dd} \cdot C_T \int_0^{T_R} \frac{dV_{out}}{dt} \, dt \]

\[ \approx V_{dd}(I_B \cdot T_R - C_T \cdot \beta) + V_{dd} \cdot C_T \cdot \alpha \]

Where, assuming \( V_o(\infty) \approx V_o(T_R) \). Fig. 4 indicates the trend of the energy consumption \( E \), which is an exponential function of the bias current \( I_B \) and the device gain factor \( K_n \).

Obviously, increasing the bias current value leads to much higher energy consumption. This is the reason why the read-out speed cannot be increased significantly just by conducting more current into the source follower. By the way, it is important to state that for a certain value of the bias current, the larger \( K_n \), the higher read-out speed. As a result, the power integration time \( T_R \) is reduced, leading to lower energy consumption. The value of \( K_n \) is mainly determined by the doping concentration and the transistor size of the source follower. It is hard to increase the transistor size, due to the limitation of the pixel area. Therefore, increasing the doping concentration is the only way to improve the performance of the CMOS image sensor. However, this requirement can only be achieved by a special CMOS process.

Another important factor which determines both the read-out speed and energy consumption is the threshold voltage of the source follower. Fig. 5 demonstrates the read-out
time and energy consumption as a function of the source follower’s threshold voltage $V_{th}$, when assuming $I_B = 1 uA$ and $K_n = 100 uA/V^2$.

$$R(C)S.N = 1 - K = 1$$  \hspace{1cm} (11)

Then, the transfer function of CDS Circuit can be derived as:

$$|H_{CDS}(\omega)| = \sqrt{2}[1 - \cos(\omega T)] \hspace{1cm} (11)$$

For an instance, the original output noise is depicted in Fig. 6 (A) and the frequency response of the CDS circuit’s transfer function $(T = 10 uS)$ is shown in Fig. 6 (B). In Fig. 6 (C), the output noise power density after the CDS circuit is demonstrated with different values of $T$.

IV. THE RELATIONSHIP BETWEEN READ-OUT SPEED AND NOISE CANCELLATION

Since the frequency counter can be performed as a CDS circuit by up-count the reset voltage and down-count the output signal.

A. The Transfer Function of CDS Circuit

When we consider the CDS is a differentiator, then the output of CDS should be $e_{0CDS}(t) = e_0(t)$'. Therefore, the Laplace transform of $e_{0CDS}$ should be equal to $s \cdot E_{0CDS}(s)$. Then, the transfer function of CDS Circuit can be derived as:

$$H_{CDS}(s) = \frac{E_0(s)}{E^r(s)} = 1 - e^{-Ts} \hspace{1cm} (9)$$

Furthermore,

$$|H_{CDS}(\omega)| = |1 - e^{-j\omega T}|$$

Then:

$$\varphi = \int_0^T 2\pi f_0 f(t) dt \hspace{1cm} (12)$$

Then, the output of the frequency counter defined by the total integrated phase $\Theta_{tot}$ can be expressed as:

$$\Theta_{tot} = \int_0^t 2\pi f_0 f(t)[1 - u(t - T)] dt = T2\pi f_e \hspace{1cm} (13)$$

Where, $f_e$ is the calculated average frequency of the VCO. $T$ is the counting period. This frequency counter integrates...
frequency counter and CDS Circuit) as shown in Fig. 8. The output noise can be reduced exponentially by reducing the time interval $T_1$.

When, assume $\omega_{eqn} = 2\pi \cdot (0.1 \text{GHz})$, then the frequency response of this equivalent band-pass filter with different value of $T_1$ could be shown in Fig. 7. It is important to note that the noise cancellation could be improved when speeding up the read-out circuit.

<table>
<thead>
<tr>
<th>$\omega T$</th>
<th>Noise$_{v}$</th>
<th>Noise$_{r}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0.1\text{GHz}$</td>
<td>$20$</td>
<td>$10$</td>
</tr>
<tr>
<td>$0.2\text{GHz}$</td>
<td>$10$</td>
<td>$5$</td>
</tr>
</tbody>
</table>

\[
|H(\omega)_{\text{casc}}| \approx \frac{4}{1 + j(\omega/\omega_{eqn})} \left| \sin\left(\frac{\omega}{2}T_1\right) \right| \left| \sin\left(\frac{1}{2}\omega T_2\right) \right|
\]

where, $T_1$ is the integration time of the frequency counter and $T_2$ is the interval of CDS Circuit between reset voltage read-out phase and signal read-out phase. Because for each complete CDS operation, the frequency counter need count twice, it is reasonable to assume that $T_2 = 2T_1$. Therefore:

\[
|H(\omega)_{\text{casc}}| \approx \frac{4}{1 + j(\omega/\omega_{eqn})} \left| \sin\left(\frac{\omega}{2}T_1\right) \sin\left(\omega T_2\right) \right|
\]

In order to find out the transfer function of this frequency counter, we can firstly assume that the input is an impulse signal $\delta(t)$. Then, the impulse response of the system could be:

\[
y(t) = \frac{1}{T} \int_0^T \delta(t) dt \cdot [u(t) - u(t - T)]
\]

The Laplace transform of $y(t)$ is as follow:

\[
Y(s) = \frac{1 - e^{-sT}}{sT}
\]

Because the transfer function of the system is equal to the impulse frequency response, then the frequency counter's transfer function is equal to:

\[
H_{freq\_coun}(s) = \frac{1}{1 + \frac{\omega}{\omega T}}
\]

\[
|H_{freq\_coun}(\omega)| = \left| \frac{\sin(\omega T)}{\omega T} \right|
\]

Clearly that, if $\omega \approx 0$ then:

\[
|H_{freq\_coun}(\omega)|_{\omega\approx0} = \left| \frac{\sin(\omega T)}{\omega T} \right|_{\omega\approx0} = 1
\]

This frequency counter working as a high-pass filter cannot significantly attenuate the low frequency noise. Such an intuition is consistent with the equation 17.

\[
C. \ \text{The Transfer Function of the Cascaded Equivalent Filter}
\]

When considering the column bus capacitance and source follower, there exits another equivalent low-pass filter, which is defined as [7]:

\[
H(\omega) \approx \frac{1}{1 + j(\omega/\omega_{eqn})}
\]

with

\[
\omega_{eqn} \approx \left[ C_{bus}(r_s + R_{eq1} + r_3) \right]^{-1}
\]

\[
R_{eq1} \approx \left[ g_m \frac{C_{bus}}{C_{bus} + C_{eq1}} \right]^{-1}
\]

Thus, the amplitude-frequency response of this cascaded band-pass pass filter (consists of the source follower, frequency counter and CDS circuit) can be expressed as:

\[
|H(\omega)_{\text{casc}}| \approx \left| \frac{4}{1 + j(\omega/\omega_{eqn})} \right| \left| \sin\left(\frac{\omega}{2}T_1\right) \right| \left| \sin\left(\frac{1}{2}\omega T_2\right) \right|
\]

After integrating the noise spectrum from 100Hz to (1910GHz for different values of the interval $T$, the output noise (after CDS Circuit and the frequency counter) as a function of $T$ is shown in Fig. 8. The output noise can be reduced exponentially by reducing the time interval $T$.
between the adjacent two sample phases. In other words, enhancing the read-out speed can significantly improve the noise performance of the APS imager. Therefore, this analysis provides a basic principle for low-noise CMOS image sensor design.

V. CONCLUSION

In this paper, the read-out circuit of a novel VCO based CMOS APS image sensor is detailed discussed. From the mathematic analysis and simulation results, the read-out speed and the energy consumption are both increased when providing more bias current for the source follower. Additionally, the read-out speed and the energy consumption strongly depend on not only the device gain factor but also the threshold voltage of the source follower. As a result, the noise cancellation performance of the CDS circuit and the frequency counter is jointly determined by all of those factors, which constitute the basic principle for high speed low-noise CMOS APS imager design.

ACKNOWLEDGMENT

This work was supported by a research grant from the Research Grant Council of Hong Kong Ref: 610507.

REFERENCES


